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High-speed communication circuits: voltage control oscillators and VCO-derived filters

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High-speed communication circuits: Voltage control oscillators and VCO-derived filters

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CHAPTER 1 GENERAL INTRODUCTION

Voltage Controlled Oscillators (VCO) and filters are essential functional blocks in digital communication systems, disk drive electronics, wireless receivers, optical receivers and microprocessors. VCOs and filters can be implemented in bipolar, BiCMOS, GaAs, SiGe and CMOS technologies. These processes provide different advantages and disadvantages. In order to get low cost and low dissipated power, which is very important in the modern market, CMOS technology becomes more and more attractive.

In this dissertation, two main topics are focused upon. The first one is the study of the high speed VCO with temperature and process variation compensation. The second one is the study of high-speed filters. Both of them are implemented in a TSMC 0.25μm CMOS process.

The current mirror is an essential building block in many analog circuits. Although CMOS processes capture the digital market, the bipolar process remains popular for high-speed application due to the very high unity-gain frequency of the bipolar transistor. This dissertation also includes a study of bipolar current mirrors and the introduction on a new high-performance mirror structure.

1.1 Dissertation Organization

The dissertation is composed of seven chapters. An overview of the basic concepts of VCO, filter and current mirror design is presented in Chapter 1. The design of high-speed voltage controlled oscillators with process and temperature compensation are discussed in Chapter 2. The design issues for high frequency VCOs, including the transfer characteristics of the VCO and methods of maximizing the VCO frequency are discussed in Chapter 3 and 4. The concept of designing high-speed VCO-derived filters is introduced in Chapter 5. The design of current mirrors with accurate mirror gain for low β bipolar transistors is discussed in Chapter 6. Finally, The general conclusions are provided in Chapter 7.

1.2 Overview of Voltage Controlled Oscillators

Voltage-controlled oscillators (VCO) are essential building blocks in microprocessors and communication system [1] [2]. Preferred requirements in the design of many VCOs are: 1) high spectral purity and low phase noise, 2) large frequency tuning range, 3) good frequency stability to the temperature and process, 4) low power consumption, 5) low fabrication cost, and 6) linearity of frequency versus control voltage for some applications.

The VCO can be implemented in both the CMOS and bipolar process. Recently, the CMOS process has captured the most integrated circuit market. In contrast to the bipolar or GaAs counterparts, CMOS technology provides three significant advantages: low power dissipation, low fabrication cost, and the possibility of integrating digital and analog circuits on one chip to improve the overall performance. These three attributes make the CMOS process more attractive than the bipolar process in microprocessors and in the communication circuits market. Although the CMOS transistor is quite slow compared to the bipolar transistor, it does achieve and will continue to achieve significant improvements in speed due to the fact that the dimensions of MOS devices will continue to scale down as process advance. The current unity-gain frequency f_t of the CMOS transistor can be expected to approach 100 GHz as the channel length is scaled down to 50nm in 2010 [3].

Three types of CMOS VCOs are commonly considerations in the design of the VCO. They are the ring oscillator VCO [2] [4], the LC tank VCO [5] [6], and the relaxation VCO [7].

The LC tank VCO often has superior spectral purity and a large tuning range. The quality of the LC-VCO relies on the high-quality LC-tank circuit. Multi-chip solutions provide high-quality reactive component, but invariably increases the fabrication costs. Although fully integrated spiral inductors on silicon substrates do not require extra post-processing steps and have found increased applications in recently years, due to the parasitic effects, only low-quality inductors can be achieved in most process. The on chip inductors also occupy a large area and thus increase fabrication costs. Recently, the bonding wire has been used as the inductor [8]. This technique increases the quality factor of the LC tank, but it is not widely accepted in industry for mass production due to yield concerns and the costs associated with providing additional bonding works.

In contrast to the LC tank, a relaxation VCO doesn't need external components so it can be fully integrated. But unfortunately, its phase noise is often inferior and the tuning range is often relatively small.

One of the most commonly used CMOS VCOs in high-speed circuits is the ring oscillator. Monolithic CMOS ring oscillators have advantages in terms of relative high spectral purity, high frequency capability, a large tuning range, good matching, multi-phase outputs and low fabrication cost.

In this dissertation, the goal is to design a high quality CMOS ring VCO. The study focuses on: 1) reducing the variation of VCO frequency to the process and temperature variations, 2) keeping a monotone relationship between the control voltage and frequency of the VCO, 3) maximizing the operation frequency of the VCO in a given process.

1.3 Overview of High - Speed Filters

Integrated analog filters can be classified into two categories: continuous-time filters and discrete-time filters. Continuous-time filters are capable of operating at higher frequencies than the discrete-time filter but at a cost of deterioration in linearity and noise performance. There are, however, many applications in the areas of signal processing circuits in which the distortion and noise performance requirements are relaxed and the integrated filters are particular attractive in these environments [9]. The design of integrated filters poses increasable challenges as the speed of the systems continues to increase.

In the discrete-time filter domain, the switch-capacitor filter is widely used. In switch -capacitor filters, the time constant and quality factor of the filter are dependent on the ratio of two passive elements. So the switch-capacitor filters have very excellent frequency linearity and accuracy. Unfortunately the speed of operation of the switch-capacitor filters is dependent on the relative lower bandwidth of the operational amplifiers and the speed of the reference clock.

In the continuous-time filter domain, g_m-C filters offer a speed advantage over active R-C and MOSFET-C filters. The speed of the active R-C and MOSFET-C filter is limited by the bandwidth of the OP AMP that is the basic active element in these filters. The speed of

the g_m-C filter is limited by the unit gain frequency of a transconductor which is much higher than the gain-bandwidth product of the OP AMP.

Reported continuous-time CMOS monolithic filters are invariably limited to operating frequency that are much lower than the reported oscillation frequencies of VCOs designed in the same process. This dissertation proposes a new type integrated filter, the VCO-derived filter. This type of filter can operate at very high frequencies.

1.4 Overview of Bipolar Current Mirror

The current mirror is one of the most basic building blocks used in linear IC design. Although the CMOS process has become dominant in applications requiring a large amount of digital circuitry on a chip, BJT circuits in either BiCMOS or bipolar processes remain popular for high-speed applications due to the very high unity-gain frequencies attainable with modern bipolar transistors. Unfortunately, in bipolar transistors, the base control terminal draws a nonzero input current. The nonzero input current causes an error in the mirror gain.

There are several known approaches for minimizing the base current effects [9]-[11]. Most are suitable for high β transistors where the detrimental effects of base current loss on mirror gain are already modest. For low β transistors, most existing methods show either poor accuracy or poor frequency response.

A new bipolar current mirror, which provides a better gain match for low β transistors is introduced in this dissertation.

CHAPTER 2 HIGH-SPEED VCO WITH PROCESS AND TEMPERATURE COMPENSATION

2.1 Problem Definition and Motivation

Recently, voltage controlled oscillators have been successfully used in high-speed clock recovery systems. One key property of any VCO is the transfer characteristics which is the relationship between the input control voltage and the frequency of the VCO. Often the transfer characteristics are nearly linear in which case the sensitivity of the VCO is a constant. For purposes of discussion herein below, the term "sensitivity" will refer to the derivative of the transfer characteristics. To facilitate the discussion, it will be assumed that the sensitivity is a constant although such an assumption is not critical. A VCO with a high sensitivity will experience large changes in the frequency due to small changes in the input control voltages whereas a VCO with a low sensitivity will experience small changes for the same changes in the input control voltage. A VCO with a high sensitivity will be more vulnerable to noise on the control voltage input. Noise on the control voltage input will cause jitter in the output signal of the VCO. When the VCO is used as part of a Phase Locked Loop in a high-speed clock or data recovery circuit, increases in jitter will degrade performance (specifically increase the error rate in the system). Jitter is one of the major obstacles that must be managed when designing high-speed serial communications networks.

Most existing VCOs used in high-speed data and clock recovery circuits are intentionally designed to have a high sensitivity. This is necessary because the VCO must be able to function properly in the presence of large variations in processing technology, variations of temperature, and variations in the frequency of the incoming data. Variations in VCO frequency due to process changes are often in the ±20% range. Correspondingly variations in VCO frequency due to temperature changes with a fixed control voltage are often in the ±20% range as well. Variations in VCO frequency due to incoming data changes are often in the ± 0.01 % to 1% range depending upon the particular protocol that is being implemented. To guarantee that the VCO will work over process variations, over temperature

variations, and over system variations, the VCO adjustment range must accommodate the cumulative deviations due to all three factors.

The following simplified example is discussed below for the demonstration of the implications of process and temperature compensation. If a system specification as specified in a standard stipulated that the frequency will be restricted to a ± 1 % variation, a process variation causes a change in VCO frequency that is bounded by ± 20 %, and a temperature variation causes a change in VCO frequency bounded by ± 20 %, then the VCO would need to be designed for ± 41 % variation. It can be seen that the system level variation is very small compared to the process and temperature variations and thus the sensitivity must be very high to accommodate for the temperature and process variations. In transceiver applications, this high sensitivity is accompanied by an increase in the jitter of the data or clock recovery circuitry. If perfect temperature and process compensation were provided, the VCO in the preceding example would need to only accommodate for the system level variation of ± 1 %. This would allow for a drastic reduction in the sensitivity of the VCO and correspondingly a substantial reduction in jitter.

2.2 Literature Review

There are several ways to provide temperature and process compensation [12]-[15]. Recent work by Wing-Hong Chan [12] discussed an attempt to reduce the jitter in Phase Locked Loops and Delay Locked Loops by providing temperature compensation of the VCO. In his design, Chan used a Proportional To Absolute Temperature (PTAT) current to achieve a temperature compensated replica biasing scheme. Figure 2.1 shows the circuits used by Chan for temperature compensated biasing. Figure 2.2 shows the block diagram of an interpolating VCO with temperature variation compensation. This provides for a reasonable level of temperature compensation, but from a system level perspective, providing only temperature compensation without process compensation does not allow for the dramatic reduction in sensitivity discussed above. On the other hand, a temperature stable resistor, which is unavailable in practical commercial CMOS process, is also needed in the Chan realization. This is another disadvantage of Chan's approach.

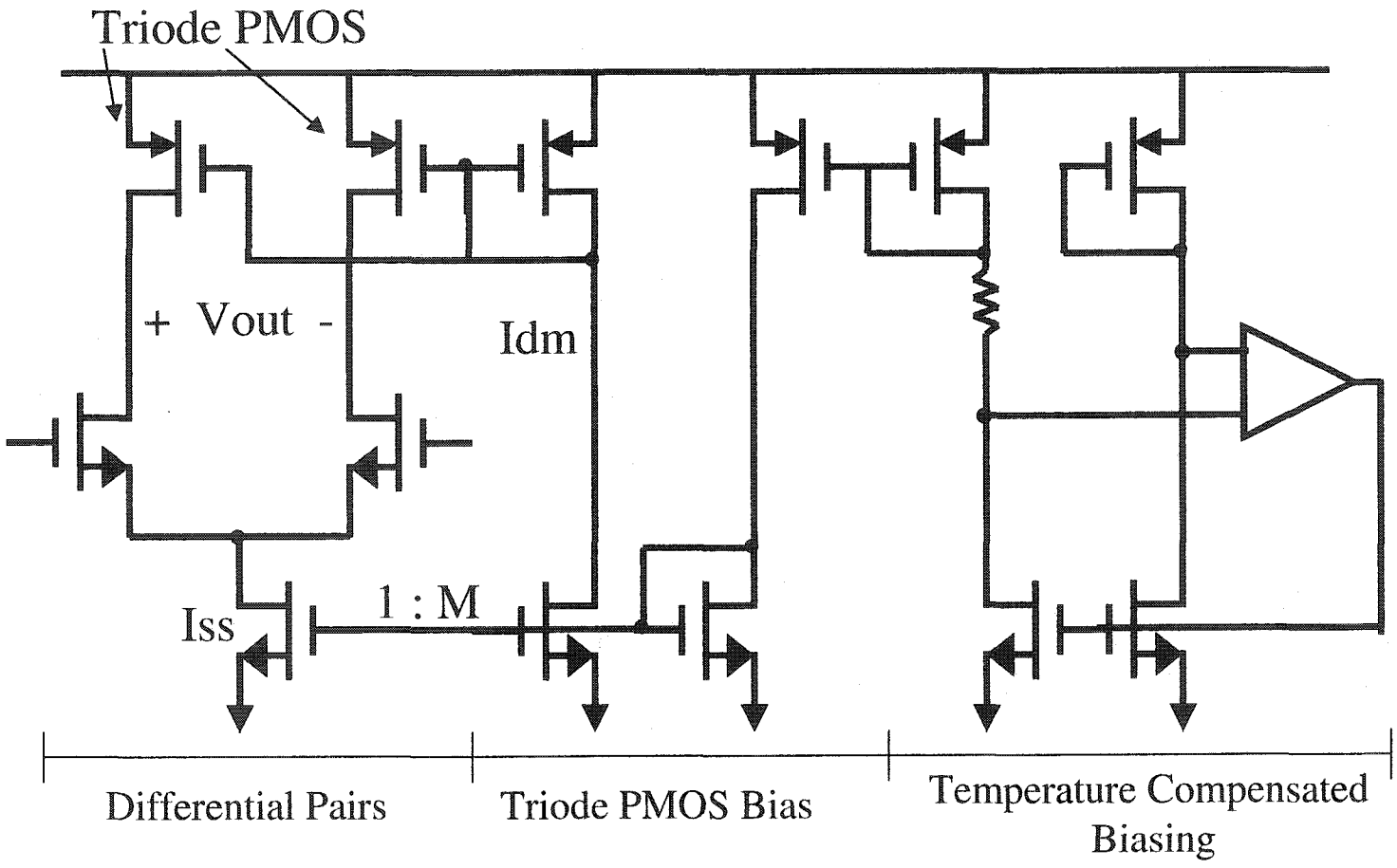


Figure 2.1: Circuits of temperature compensated biasing

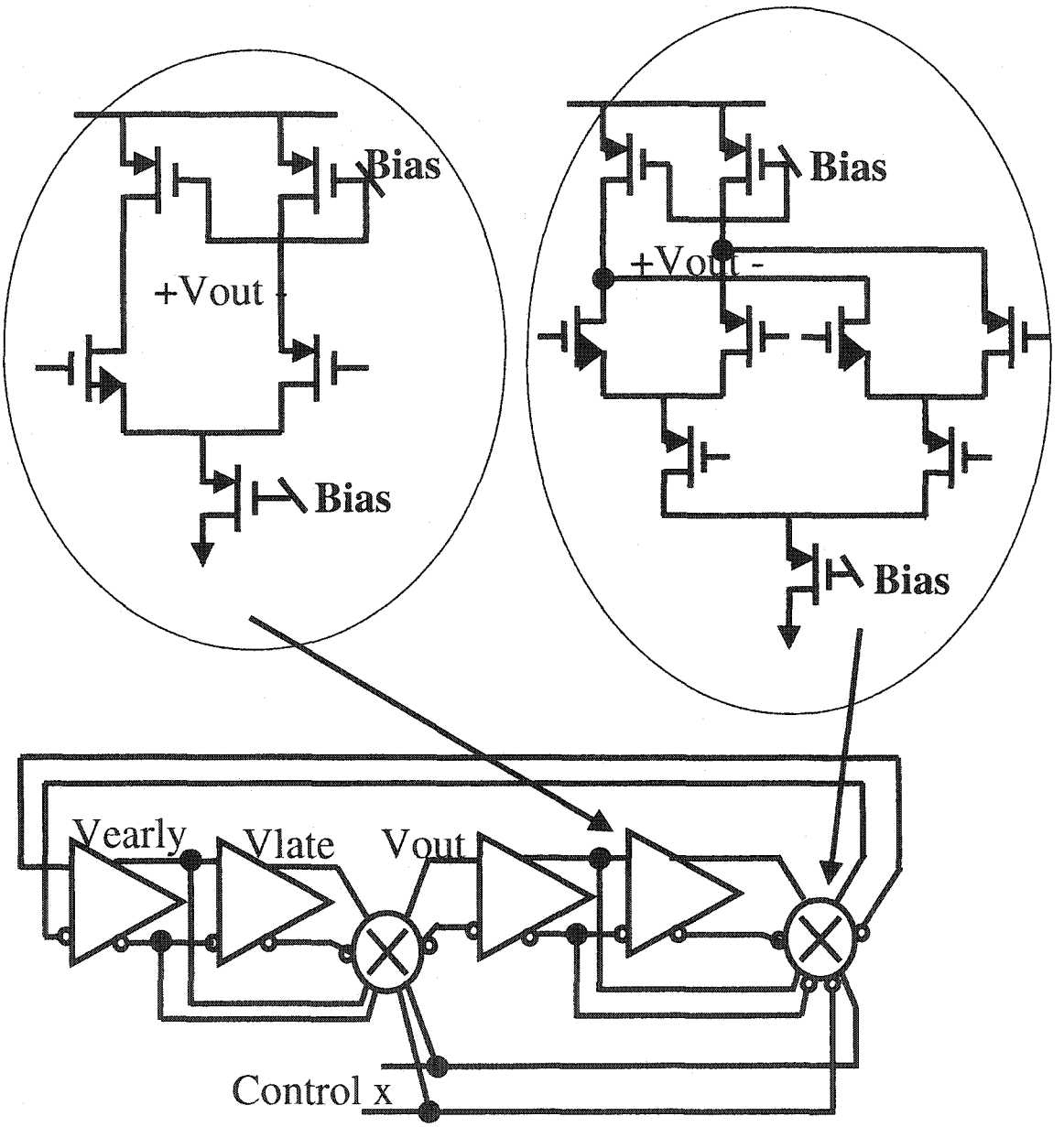


Figure 2.2: Block diagram of an interpolating VCO

2.3 VCO with Process and Temperature Compensation Design

Our strategy provides for both temperature and process compensation and thus offers potential for a major reduction in the sensitivity of the VCO. This goal is achieved by using a master-slave approach in which a master VCO is compensated for process and temperature variations. The master VCO is embedded in a Phase Locked Loop (PLL) which is locked to a reference frequency. The bandwidth of the loop filter in the PLL can be made very narrow because there are no process variations once fabrication is complete and because thermal variations have very long time constants relative to the period of the incoming data. The control signal of each VCO is comprised of two additive parts. One is controlled by a temperature and process compensation bias circuit and the other is controlled by an external input. If the reference frequency input of the PLL is temperature and process independent, the control voltage of the master VCO in the PLL will track the temperature and process variations. This control voltage is fed to the slave VCO. If the two VCOs are nominally matched (or have matched internal delay cells), the compensating voltage that is needed to compensate the master VCO for temperature and process will also approximately compensate the slave VCO for temperature and process. Thus, the external control input ideally need not compensate for either temperature or process variations and thus must only compensate for system level variations. As such, the sensitivity to the incoming data variation of the slave VCO can be made very small resulting in a reduction of jitter in data and clock recovery circuits that use the slave VCO.

2.3.1 The architecture of our proposal design

The block diagram of a temperature and process compensated VCO system is shown in Figure 2.3. The PLL is comprised of three basic elements, a Phase-Frequency Detector (PFD), a Loop Filter (LF) and a master VCO (VCO1). The system includes two VCOs, VCO_1 (master) and VCO_2 (slave). The two VCOs have the same delay stages. Each delay stage has two summed control inputs: one from the output of the loop filter V_{ctrl} and the other from an external input through V_{x1} (V_{x2}). The VCOs must have a large tuning range and gain from the V_{ctrl} input to compensate for process and temperature variations.

The operation of this system will be described by first assuming that the external inputs to the VCOs, V_{x1} and V_{x2}, are the same. Since process variations show no time dependence and thermal variations inherently have very large time constants relative to the frequency of oscillation of either the master VCO or the slave VCO, the time constant of the loop filter can be made very long but get short relative to the thermal time constants. This will provide good noise immunity as well as temperature and process compensation for the frequency of oscillation of the VCOs.

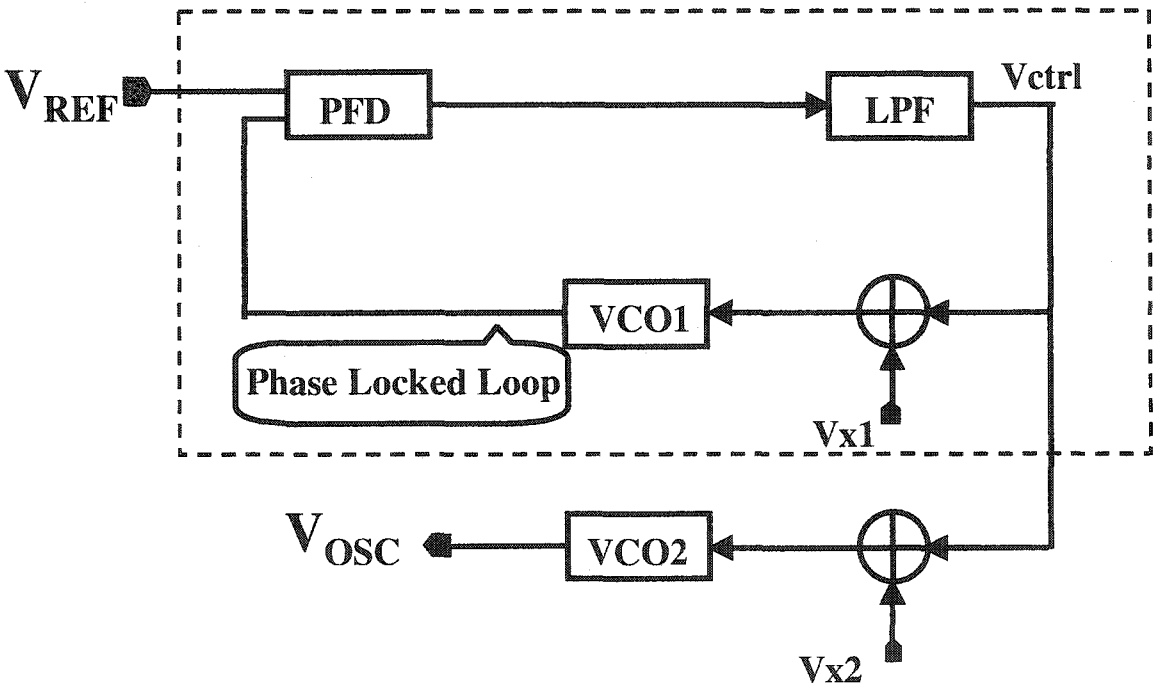


Figure 2.3: Basic architecture of temperature and process compensation VCO

Process and temperature compensation for the slave VCO (VCO2) can be achieved if the process and temperature dependencies of the delay stages in the slave VCO (VCO2) are similar to or identical to those in the master VCO (VCO1). One way to achieve similar process and temperature dependencies between VCO1 and VCO2 is to use identical delay stages in both structures. The oscillating frequencies of these VCOs can be made different if the number of delay stages in these structures differs. If the number of stages were the same, the temperature and process variations will be nearly the same, differing slightly due to

random mismatch effects and small thermal gradients across the die. If the number of stages differ, the wave shape and signal levels will vary somewhat at high frequencies thus introducing some variations in the process and temperature dependencies between the delay stages of VCO1 and VCO2. These variations will manifest themselves in incomplete compensation of VCO2 by the control signal Vctrl.

The V_{x1} input to VCO1 ideally has no impact on the compensation characteristics of the PLL provided linear operation of the three blocks of the PLL is maintained. It is provided to facilitate obtaining architectural symmetry between the delay stages in the VCOs. The V_{x2} input to VCO2 will serve as the control input to VCO2. The gain of the VCO (freq./V_{x2}) can be made very small. This low VCO gain is desirable for reducing jitter in high-speed communication circuits where the slave VCO is used in a high frequency PLL for clock and data recovery.

2.3.2 Implementation in TSMC 0.25 μM CMOS process

The high-frequency implementation will be focused on systems where the nominal operating frequency of the slave VCO is 2GHz and where the maximum variations required on the slave VCO output is at most ± 1%. Since a data rate variation of ± 0.01% to 1% is typical of what is seen in standards for high-speed data communication networks [16], a VCO with this narrow adjustment range should be useful for building low-jitter clock and data recovery transceivers.

A specific implementation of the system of Figure 2.3 is shown in Figure 2.4. The delay stages in the VCOs are fully differential input and output stages with both current source and load biasing. The PFD provides both an UP signal and a DOWN signal to the Loop Filter. The Loop Filter is comprised of three blocks: a Charge Pump (CP) that converts the UP and DOWN phase voltage information into a single-ended current, a Low-Pass Filter that filters this current to generate a control voltage, and a Self-Bias Generator that converts the filter output voltage to the two reference voltages that bias the delay stages.

The design was implemented in a TSMC 0.25 μm process that is available through the MOSIS program. The details of the following design discussions are applicable specifically to that process.

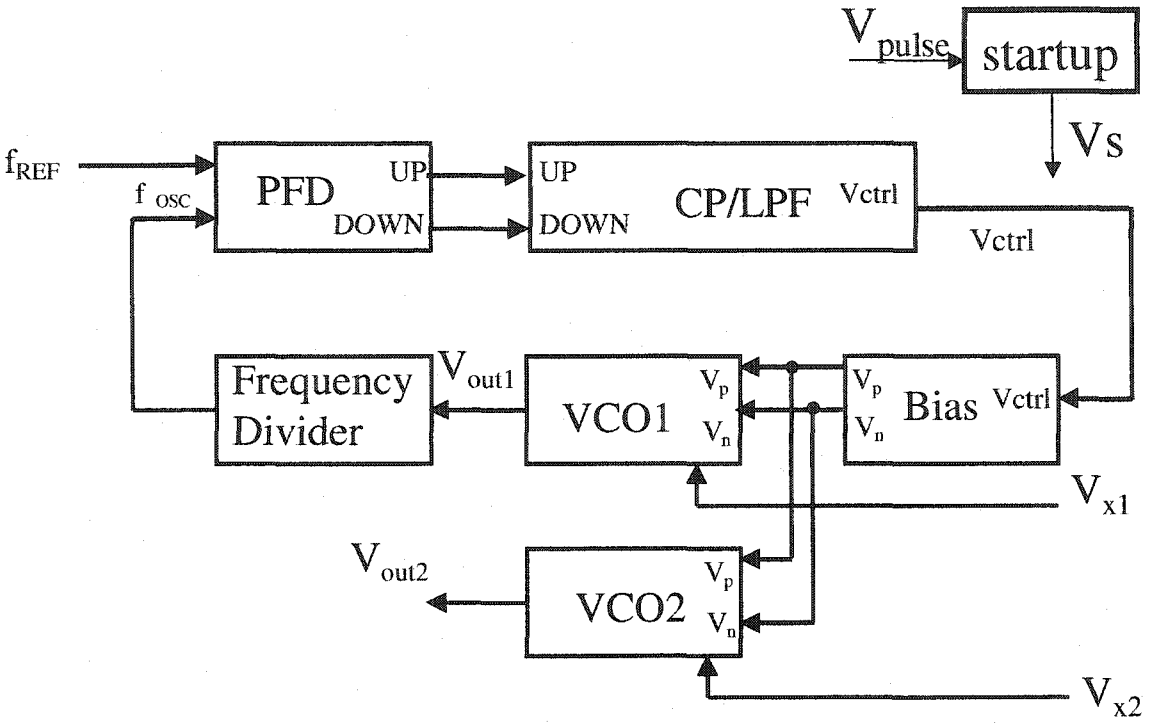


Figure 2.4: Block diagram of temperature and process compensation VCO in 2 GHz implementation

2.3.2.1 Review of Charge-Pump Phase Locked Loop (CPPLL) Design

The basic PLL is comprised of four parts, a frequency detector (PD), a low-pass filter (LF), a VCO and a frequency divider. The PD compares the phase of the VCO divided output and a reference signal, generating an error signal that is used to adjust the VCO frequency until the phase error is time constant. The PLL is locked when the phase error is constant over time. i.e., when the loop is locked, the VCO will generate an output with a frequency equal to that of the reference input

In many high-speed communication systems, a crystal-referenced clock is generated that is at a much lower frequency than the data rate of the system. These crystal-referenced clocks are inherently very temperature stable and nearly independent of the parameters of a process. It will be assumed that such a clock is available and it is used to generated the reference signal V_{REF} in the phase locked loop The exact frequency of the clock is not critical, only the temperature and process insensitivity of the clock.

The locking process of the PLL is highly nonlinear. Fortunately, once a PLL is in lock, its dynamic response to input-signal phase and frequency changes can be well approximately by a linear model, as long as these changes are slow and small around their operation point [9] [17].

I will consider two types of PLLs [17]. A type I PLL has one pole at the original in the open loop transfer function. The pole comes from the VCO because the VCO integrates the phase error between the periodic reference input and the VCO output. For convenience, it will be assumed that the loop filter is a first-order low-pass filter although such an assumption is not necessary. With this assumption the type I PLL is a second-order system Figure 2.5 [17] shows the linear model of the type I PLL where ω_{LPF} is the -3 dB bandwidth of the low-pass filter. The open loop transfer function of the PLL is

$$H(s)\Big|_{open} = K_{PD} \bullet \frac{1}{1+\dfrac{s}{\omega_{LPF}}} \bullet \frac{K_{VCO}}{s} \tag{2.1}$$

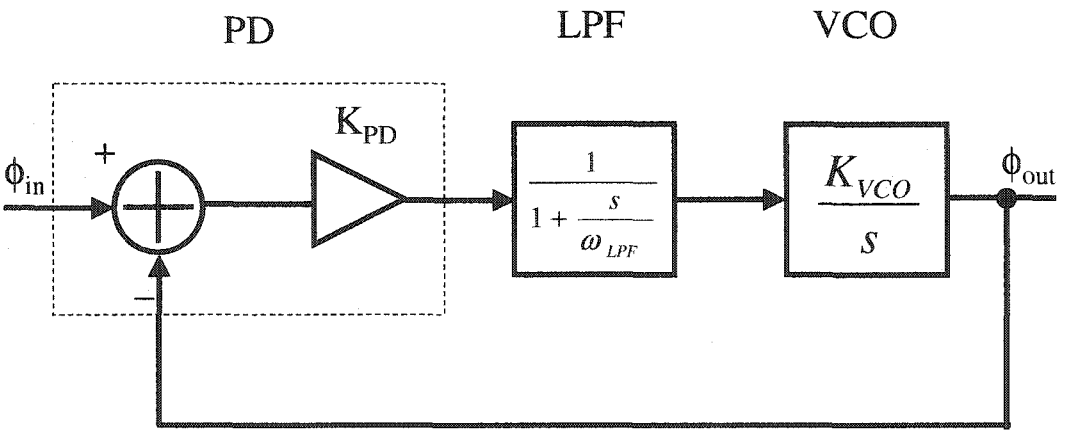


Figure 2.5: The linear model of type I PLL

The closed-loop transfer function is

$$H(s)\Big|_{closed} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} \tag{2.2}$$

As expected, when s → 0, $H(s)|_{closed} \rightarrow 1$. Equation (2.2) reveals the fact that when the input phase changes very slowly, the output phase will follow the input phase change. The natural frequency of the loop and damping factor is given in Equation (2.3) and (2.4)

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \tag{2.3}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}} \tag{2.4}$$

An important observation from Equation (2.4) is that the damping factor of the loop decreases as the PD gain K_{PD} and the `VCO gain K_{VCO} increase. On the other hand, as ω_{LPF} is reduced to minimize the ripple on the control voltage, the damping factor degrades also.

The two poles of the closed-loop system are given by

$$s_{1,2} = \left(-\varsigma \pm \sqrt{\varsigma^2 - 1}\right)\omega_n \tag{2.5}$$

If $\varsigma > 1$, both poles are real, the system is over damped, and the transient response contains two exponentials with time constants $1/s_1$ and $1/s_2$, If $\varsigma < 1$, the poles are complex and the response to an input frequency step $\omega_{in} = \Delta\omega u(t)$ is equal to

$$\omega_{out}(t) = \left[1 - \frac{1}{\sqrt{1-\varsigma^2}}e^{-\varsigma\omega_n t}\sin\left(\omega_n\sqrt{1-\varsigma}\ t + \theta\right)\right]\Delta\omega u(t) \tag{2.6}$$

where ω_{out} is the change in the output frequency and $\theta = \sin^{-1}\sqrt{1-\varsigma^2}$. Thus, the step response contains a sinusoidal component with a frequency $\omega_n\sqrt{1-\varsigma^2}$ that decays with a time constant $(\varsigma\omega_n)^{-1}$.

Equation (2.6) indicates that the exponential decay determines how fast the output approaches its final value, implying the settling speed of PLL is proportional to $\zeta\omega_n$.

From Equation (2.3) and (2.4), we have Equation (2.7)

$$\zeta\omega_n = \frac{1}{2}\omega_{LPF} \,,. \tag{2.7}$$

A type II PLL is also called a Charge Pump PLL (CPPLL). In our design, a CPPLL is chosen. The basic CPPLL includes a Phase Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter, and a VCO. Figure 2.6 shows a block diagram of a CPPLL and Figure 2.7 shows the linear model of a CPPLL[17]. Neglecting the capacitor C_2 first, the open loop transfer function is shown in Equation (2.8).

$$H(s)\Big|_{open} = \frac{I_P}{2\pi} \bullet \left(R_p + \frac{1}{C_p s} \right) \bullet \frac{K_{VCO}}{s} \tag{2.8}$$

The closed-loop transfer function is described by Equation (2.9)

$$H(s)\Big|_{closed} = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi} K_{VCO} R_P s + \frac{I_P}{2\pi C_P} K_{VCO}} \tag{2.9}$$

The natural frequency of the loop and the damping factor are

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}} \tag{2.10}$$

$$\zeta = \frac{R_p}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}} \tag{2.11}$$

An observation from Equation (2.11) is that the stability of the loop becomes worse as $I_p K_{VCO}$ decrease.

With complex poles, the decay time constant is give $1/(\zeta\omega_n) = 4\pi/(R_p I_p K_{VCO})$. This means that the greater $I_p K_{VCO}$, the faster of the settling time of the loop.

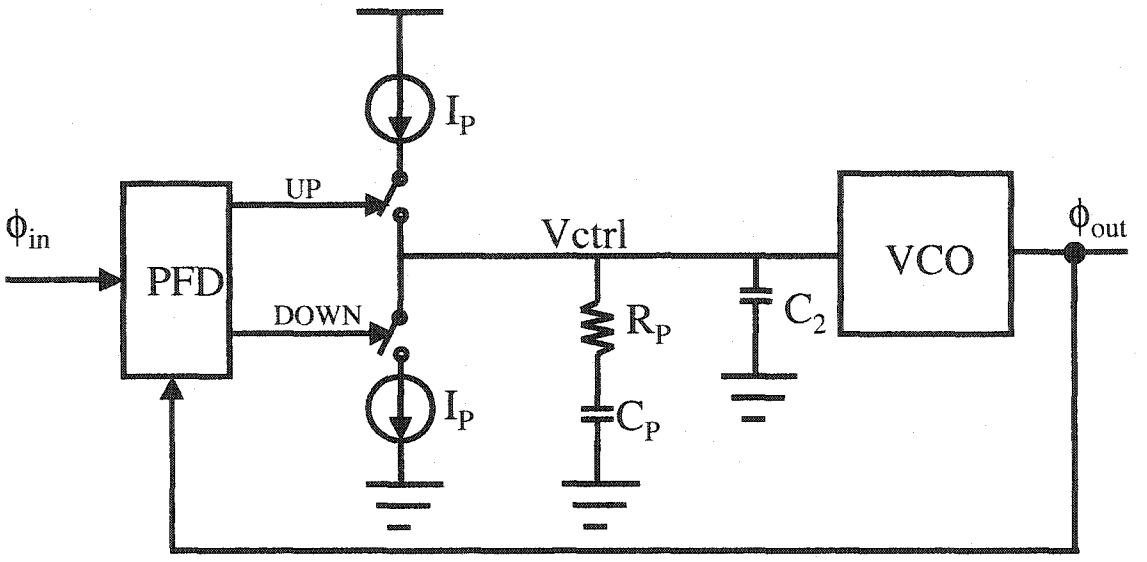


Figure 2.6: Simple Charge Pump PLL

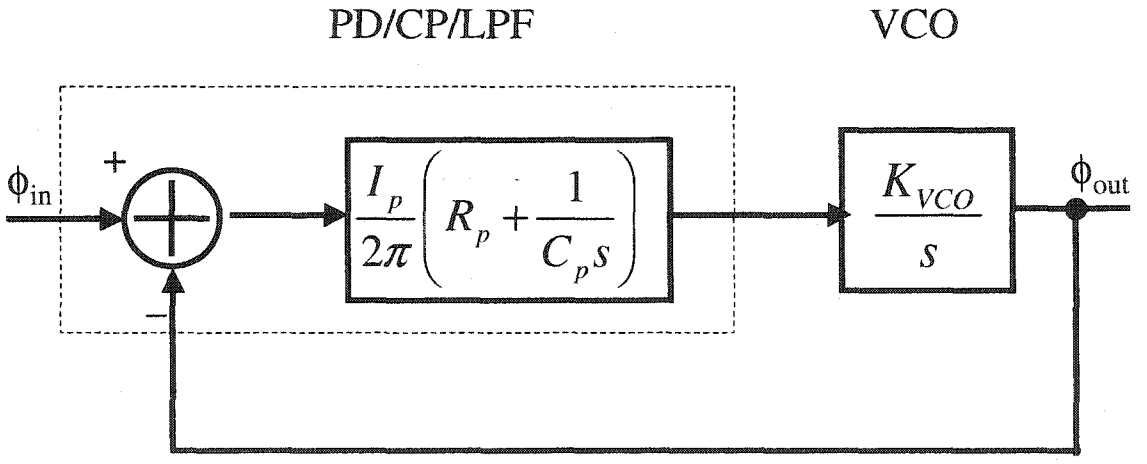


Figure 2.7: The linear model of simple Charge Pump PLL

The zero $s_z = -1/(R_p C_p)$ in the loop filter makes the loop stable. But when the Charge Pump current charges or discharges the loop capacitor, it will cause the node voltage ripple The voltage ripple modulates the VCO frequency, producing a waveform that is no longer periodic, i.e. causing a jitter at the output signal. A small capacitor C_2 is added to minimize the ripple. After the small capacitor added, the PLL is a third-order system. But, if the second capacitor is relatively smaller compared to the first one (less than one of tenth),

the PLL can be approximated in a second-order system. And all discussions above can be applied [18].

The most important issue when designing a PLL is its jitter performance. For CPPLL, there are four main jitter sources: the supply and ground noise, the substrate coupled noise, the device noise and the input jitter in a reference (or input data). The non-idealities of the building block in the CPPLL will also cause the phase jitter. These phenomena will be discussed in detail later.

2.3.2.2 VCO delay stage design

The delay stage used in both the master VCO (VCO1) and the slave VCO (VCO2) is shown in Figure 2.8. The temperature and process compensation is provided by the control voltages, V_P and V_N. Since process and temperature compensation which requires a large delay adjustment range is already provided by V_P and V_N, the small delay adjustment range provided by Vx will require only a small change in the tail current. This can be achieved by making M8 small compared to M7.

Equation (2.12) gives an approximate expression for the delay of the delay stage in terms of the total tail current.

$$T_d = \frac{C_{eff}}{\sqrt{2 * k * I_{tail}}} \tag{2.12}$$

where T_d is the average delay of the high to low plus the low to high transition times, C_{eff} is the effective capacitance at the output nodes of the delay stage, I_{tail} is the differential pail tail current, and $k = \frac{\mu C_{ox} W_1}{L_1}$. Here we assume that the input transistors M1 and M2 are in the saturation region so the small signal approximation can be used.

Since I_{tail} is the sum of the current through M7, I_{tailn}, and the current through M8, I_{tailx}, the delay can be expressed as

$$T_d = \frac{C_{eff}}{\sqrt{2 * k * (I_{tail\,n} + I_{tailx})}} \tag{2.13}$$

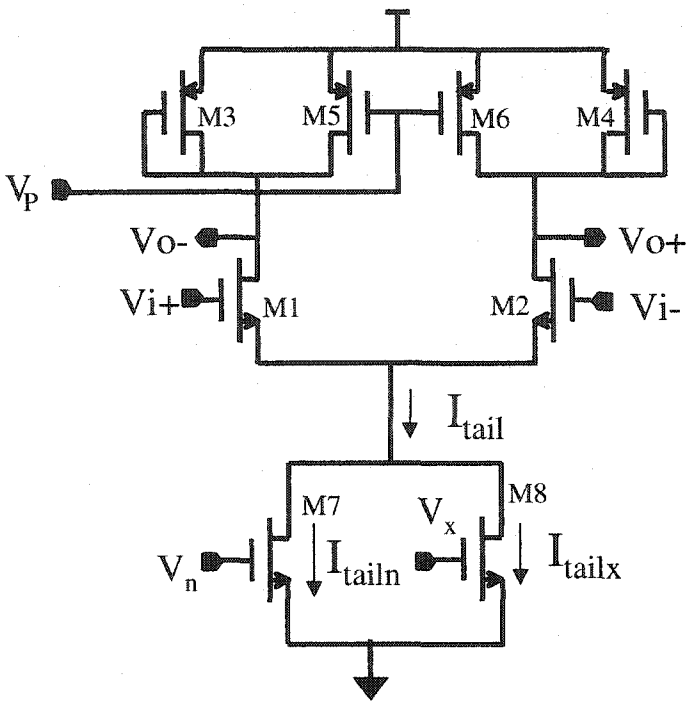


Figure 2.8: Delay stage of the VCO

If the percent change in the delay due to the change of the current I_{tailx} is assumed to be small and if L7 and L8 are assumed to be the same, the change in delay can be given as

$$\frac{\Delta T_d}{T_d} = \frac{\Delta I_{tailx}}{I_{tail}} = \frac{2*W_8*V_{EB8}*\Delta V_x}{W_7*V_{EB7}^2} \tag{2.14}$$

where V_{EB} is the excess bias voltage of M7 and M8.

This percentage change in delay must be provided over all temperature and process variations. It thus follows that

$$\frac{W_8}{W_7} = \frac{T_d}{\Delta T_d} * \frac{2*V_{EB8}*\Delta V_x}{V_{EB7}^2} \tag{2.15}$$

The delay cell was designed for a nominal delay of T_d = 62.5 psec. This delay was chosen so that we could build a 2GHz oscillator with four delay stages in the 0.25μm process.

Table 2.1 shows the transistors sizes of delay cell shown in Figure 2.8.

Table 2.1: The transistors sizes of the delay stage in Figure 2.8

W1/L1	W2/L2	W3/L3	W4/L4
6u/250n	6u/250n	3.5u/250n	3.5u/250n
W5/L5	W6/L6	W7/L7	W8/L8
3.5u/250n	3.5u/250n	20u/250n	2u/250n

2.3.2.3 VCO design

Figure 2.9 shows the VCO structure along with the output buffer. The output buffer provides a differential to single-ended conversion and isolates the influence of any loading from the frequency of oscillation of the VCO. The buffer structure is shown in later.

The 4-stage ring Oscillator provides complimentary in-phase and quadrature outputs. This is very attractive in monolithic communication circuits.

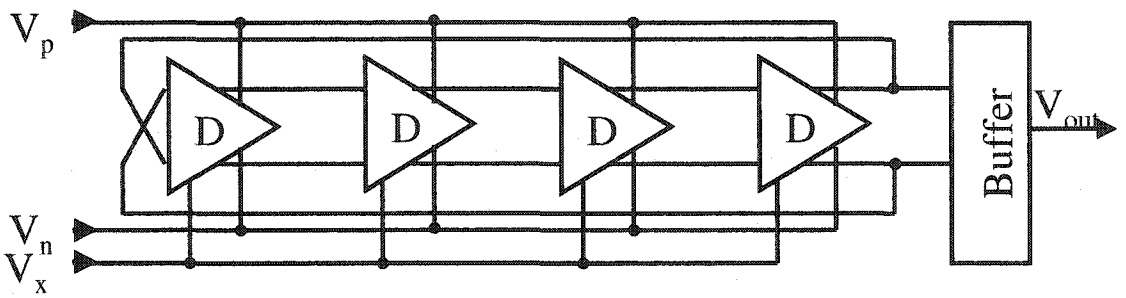


Figure 2.9: Block diagram of VCO

2.3.2.4 Phase and Frequency Detector (PFD)

The Phase Frequency Detector (PFD) used in the Figure 2.4 is shown in Figure 2.10 [2]. This detector is a rising-edge detector that generates UP and DOWN pulses on the rising edges of f_{REF} and f_{OSC}. The gate sizes in the UP path are the same as those of corresponding gates in the DOWN path.

If f_{REF} leads f_{OSC}, the UP pulse is wider than the fixed DOWN pulse with the UP pulse width being linearly dependent upon the amount of phase lead. If f_{OSC} lags f_{REF}, the DOWN pulse is wider than the fixed UP pulse with the DOWN pulse width being linearly dependent upon the amount of phase lag. When the PLL is locked, the UP and DOWN pulses have the same widths.

Figure 2.11a shows the relationship between the ideal UP and DOWN pulses when f_{REF} leads f_{OSC}. In this figure, we actually show a frequency difference as well. For the purpose of explanation the amount of phase lead indicated grossly over exaggerates what would be anticipated if the phase locked loop were in or near to lock. From this figure, the fixed down pulse width and growing up pulse width are apparent. Figure 2.11b shows the corresponding relationship when f_{REF} lags f_{OSC}.

Figure 2.11c shows an expanded view of the four pulses in the vicinity of the UP transitions in the case where f_{REF} leads f_{OSC}. The corresponding situation when f_{REF} lags f_{OSC} should be apparent. In this figure, D_T is the phase lead of f_{REF}, t_{UO} is the delay from the rising edge of the f_{OSC} pulse until the down pulse becomes high, t_{UR} is the delay from the rising edge of the f_{REF} pulse until the UP pulse becomes high, t_{UP} is the width of UP pulse, and t_{DOWN} is the width of DOWN pulse.

It follows from this figure that, when f_{REF} leads f_{OSC}, the UP and DOWN pulse widths are given by

$$t_{UP} = D_T + t_{UO} - t_{UR} + t_9 + t_{10} + t_{7u} \tag{2.16}$$

$$t_{DOWN} = t_9 + t_{10} + t_{7d} \tag{2.17}$$

where

$$t_{UR} = t_{5u} + t_{6u} + t_{7u} + t_{8u} \tag{2.18}$$

$$t_{UO} = t_{5d} + t_{6d} + t_{7d} + t_{8d} \tag{2.19}$$

And where the terms t_{ij}, $i=\{1, \ldots 8\}$,$j= \{u,d\}$ refer to the low to high delay of the ith logic gate in either the up or down path. The delays of gates numbered 9 and 10 are common to both the UP and DOWN and thus carry only a single numbered subscript.

Correspondingly, when f_{REF} lags f_{OSC}, the UP and DOWN pulse widths are given by

$$t_{UP} = t_9 + t_{10} + t_{7u} \tag{2.20}$$

$$t_{DOWN} = D_T + t_{UR} - t_{U0} + t_9 + t_{10} + t_{7d} \tag{2.21}$$

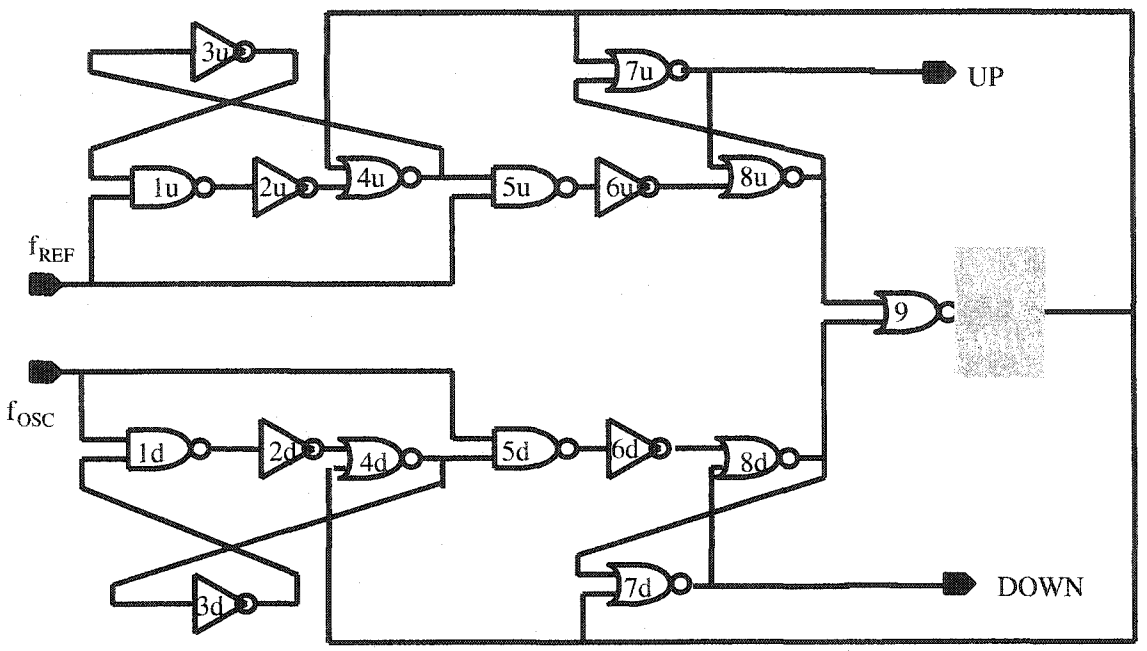


Figure 2.10: Block diagram of the PFD

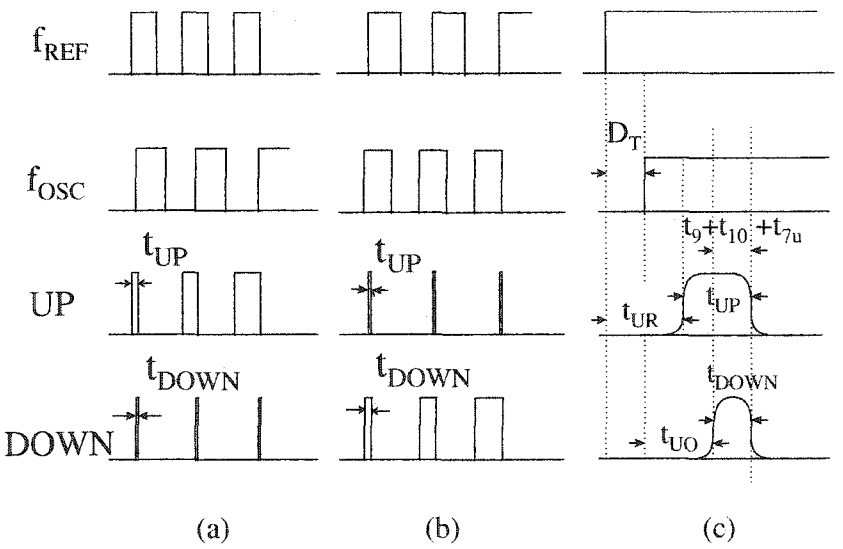


Figure 2.11: UP and DOWN waveform. (a) rising-edge of f_{REF} leads that of f_{OSC}. (b) rising edge of f_{REF} lags that of f_{OSC}. (c). expanded view in the vicinity of the UP transitions in the case when f_{REF} leads f_{OSC}

2.3.2.5 Charge Pump (CP)

A Charge Pump used in Figure 2.4 is shown in Figure 2.12. Table 2.2 shows the transistors sizes of the CP. The Charge Pump is used to convert the logical signals from the PFD into analog signals for controlling the VCOs. Ideally, when UP is active, the Charge Pump discharges the capacitors by mirroring the current *Icp* to the output as a sinking current for the duration of the UP pulse. Correspondingly, when DOWN is active, the Charge Pump charges the capacitors by mirroring *Icp* to the output as a sourcing current for the duration of the DOWN pulse.

Narrow UP or DOWN pulses cause problems with the Charge Pump. For example, if the DOWN pulse is too narrow, the delays through the Charge Pump will preclude having any sourcing current reach the filter capacitors. As a result, the Charge Pump will not respond to small phase delays between f_{REF} and f_{OSC}. This will create an apparent "dead-zone" region in the output from the phase detector. Although in such situations the phase information is not lost by the phase detector, it is not transmitted to the Charge Pump. With no corrective action taking place when the "dead-zone" exists, jitter between f_{REF} and f_{OSC} will be generated.

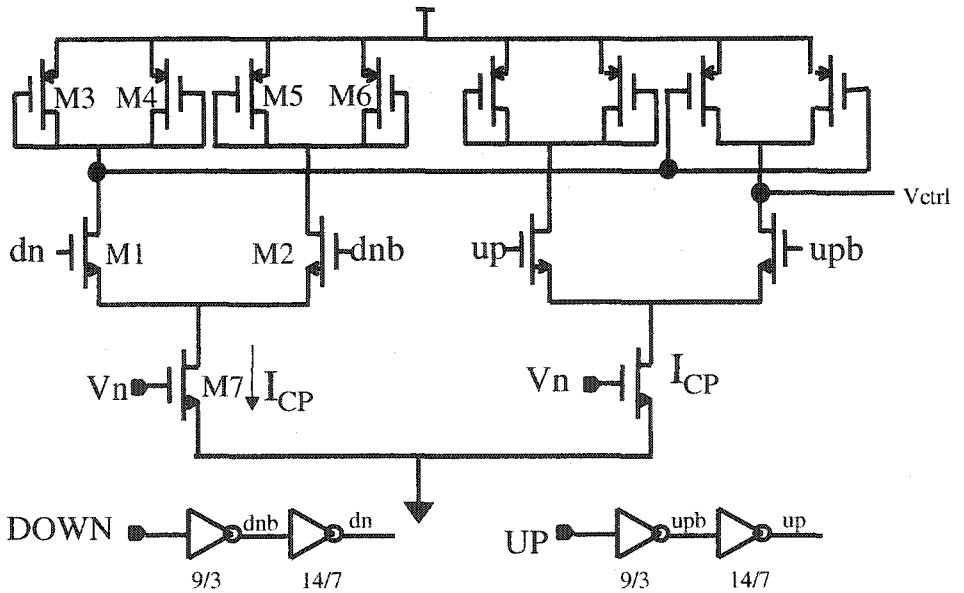


Figure 2.12: Schematic of the Charge Pump

Table 2.2: The transistors sizes of the Charge Pump in Figure 2.12

W1/L1	W2/L2	W3/L3	W4/L4
2.26u/250n	2.26u/250n	1.32u/250n	1.32u/250n
W5/L5	W6/L6	W7/L7	
1.32u/250n	1.32u/250n	7.52u/250n	

The logic gates were initially sized as minimum size. With this gate sizing, the gates had sufficiently fast response time to create a substantial "dead zone" as shown in the simulation of Figure 2.13a. Although shown only in the first quadrant, this transfer characteristic is symmetric into the third quadrant for the phase lag case as well. This dead zone covers a range of nearly ± 15 degrees.

From Equation of (2.18) to (2.21), one easy way to address the "dead zone" problem can be developed. Since t_{10} is common to both the widths of the fixed UP pulse and the fixed DOWN pulse, increasing t_{10} will reduce or eliminate the "dead zone". Since Gate 10 is formed by 2 inverters, increasing t_{10} by increasing the ratio between the two inverter stages results in the improvements shown in Figure 2.13b. Due to the mismatch between the charge and discharge currents when the UP and DOWN have identical pulse widths, the curve does not pass through the origin. The mismatch between the charge and discharge currents will cause a phase error. To eliminate this phase error, careful design and layout of the Charge Pump are required.

2.3.2.6 Loop filter

The loop filter used in Figure 2.4 is show in Figure 2.14. To implement the big capacitors, the NMOS transistors were used. The transistors size of C1 is 100um*300um and C2 is 50um*10um. From Equation (2.11) of section 2.3.2.1, the nature frequency of the PLL loop is around 2 MHz and damping factor is around 0.7.

2.3.2.7 Bias Generator

The CP generates only one control voltage for the VCO. In VCO delay cell, two control voltages are required for tuning of the VCO operation frequency. A bias generator is used to generate two control voltages from the one control voltage V_{ctrl} of Figure 2.4. A self-

bias structure is used to reduced the process and temperature variation and also provide good supply noise rejection [19] [20]. Figure 2.15 shows the schematic of the bias generator. Table 2.3 shows the transistors sizes of the bias generator. The wide-swing op amp is used to increase the input control voltage (V_{ctrl}) swing and its structure is shown in Figure 2.16. Table 2.4 shows the transistors sizes of the op amp. A capacitor of 3pf was added at the output of op amp Vn to compensate the op amp. This capacitor is implemented by CMOS transistors.

2.3.2.8Output Buffer

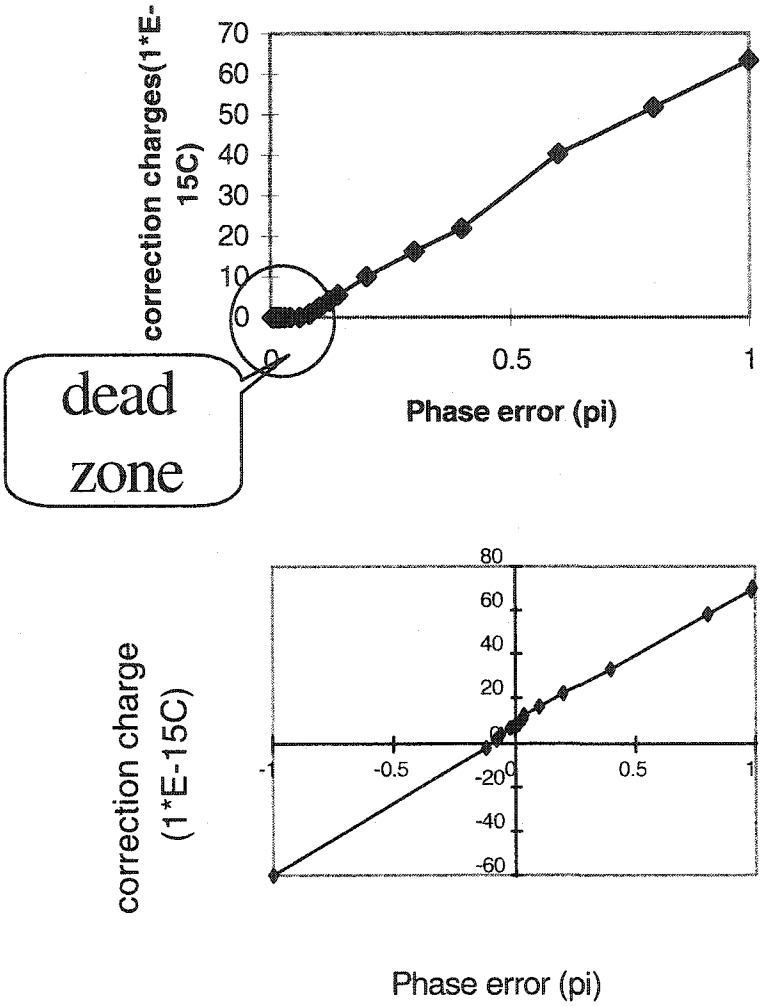
The output buffer in Figure 2.4 is show in Figure 2.17. The output buffer serves two purposes. It provides a fully differential to single-ended conversion and isolates the influence of any loading from the frequency of oscillation of the VCO. Table 2.5 shows the transistors sizes of the output buffer.

Table 2.3: The transistors sizes of the self-bias generator in Figure 2.15

W1/L1	W2/L2	W3/L3	W4/L4
6u/250n	12u/250n	3.5u/250n	3.5u/250n
W5/L5	W6/L6	W7/L7	W8/L8
7u/250n	7u/250n	20u/250n	40u/250n

Table 2.4: The transistors sizes of the op amp in Figure 2.16

W1/L1	W2/L2	W3/L3	W4/L4
40u/500n	40u/500n	2.5u/500n	2.5u/500n
W5/L5	W6/L6	W7/L7	W8/L8
40u/500n	12u/500n	12u/500n	30u/250n
W9/L9	W10/L10	W11/L11	W12/L12
30u/250n	3u/250n	30u/250n	2.5u/500n
W13/L13	W14/L14	W15/L15	
2.5u/500n	40u/500n	3u/250n	



(b)

Figure 2.13: Phase error transfer characteristic of the VCO (a) without delay gate 10 in PFD, (b) with delay gate 10 in PFD

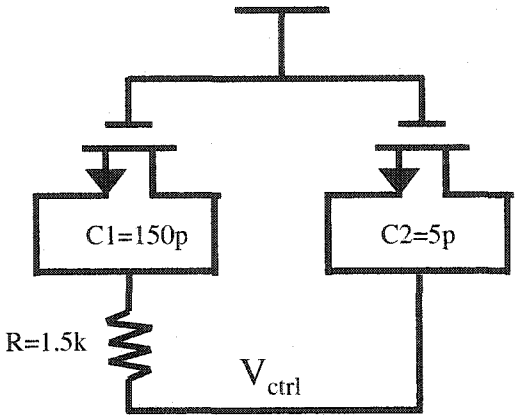


Figure 2.14: Schematic of loop filter

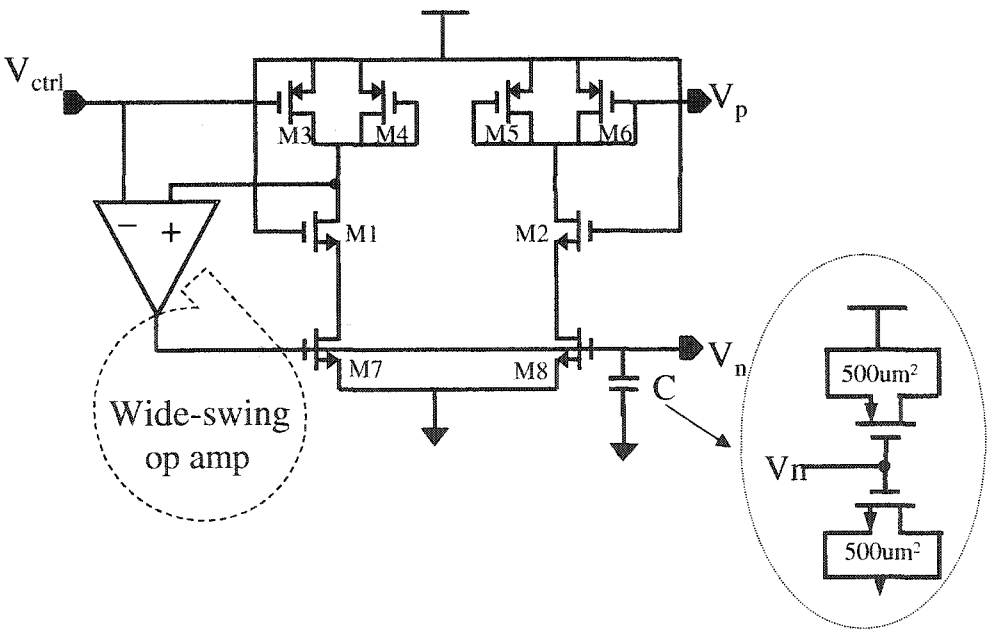


Figure 2.15: Schematic of the self-bias generator

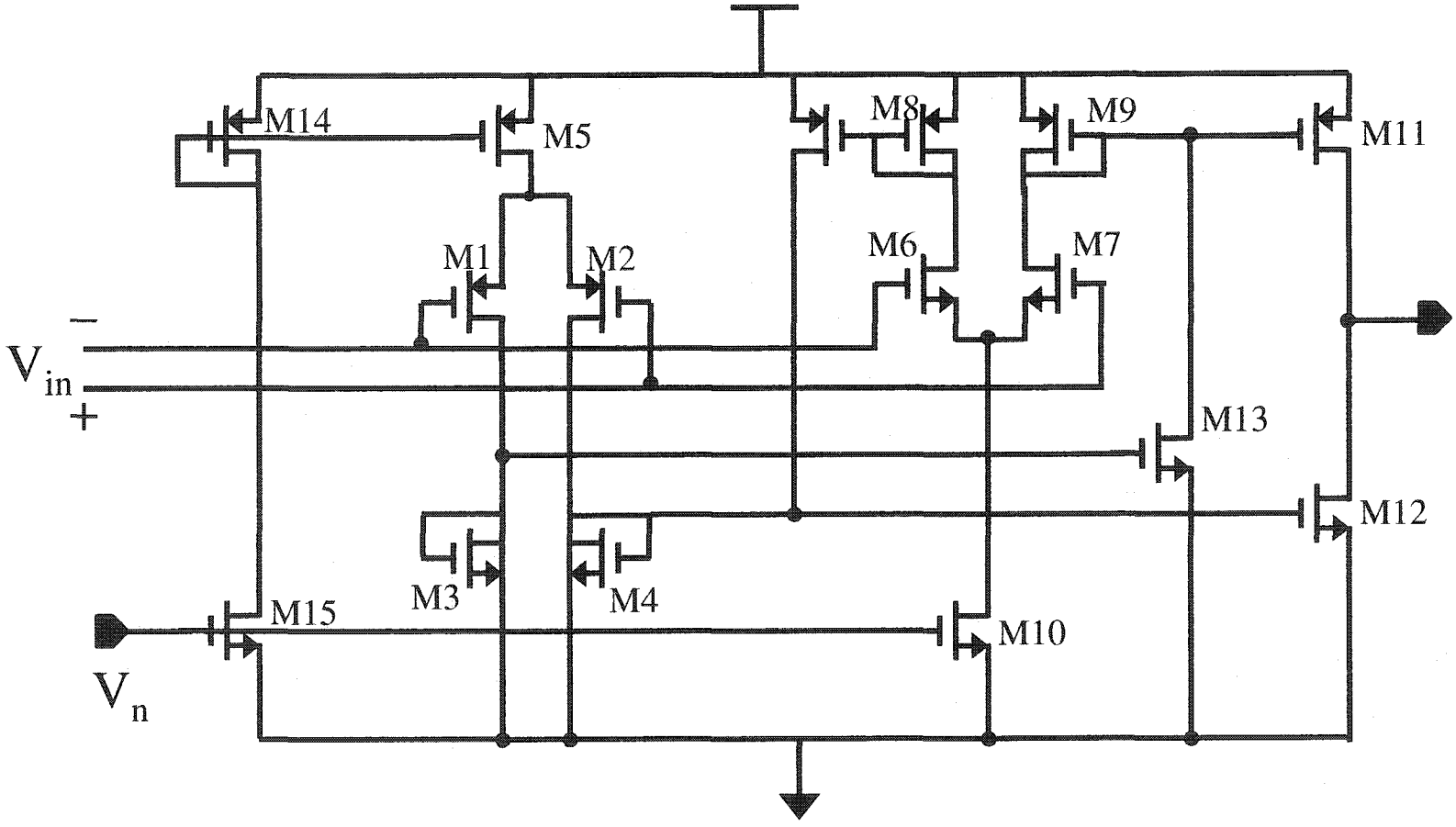


Figure 2.16: The schematic of the wide-swing OPAMP

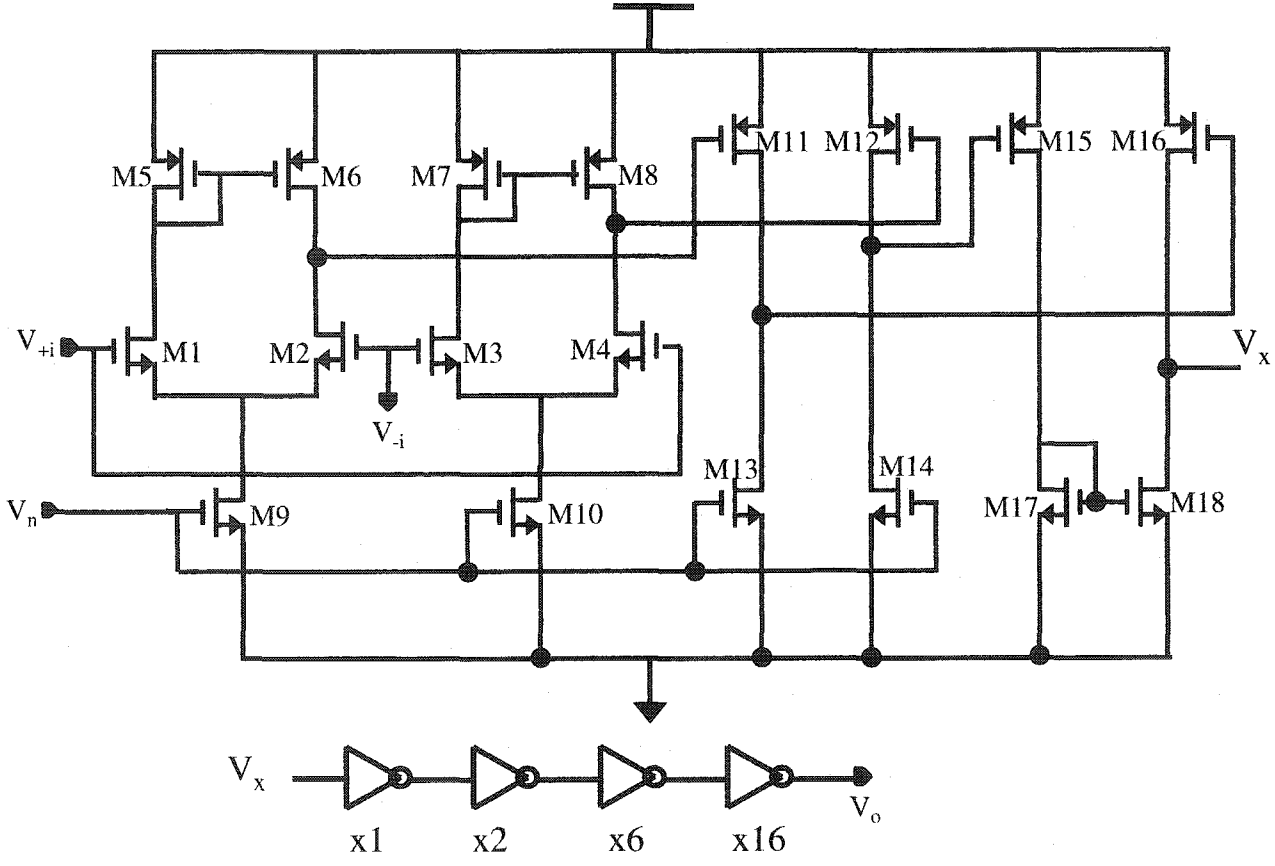


Figure 2.17: The schematic of the output buffer.

2.3.2.9 Frequency Divider

The Frequency Divider show in Figure 2.4 is used to divide the output frequency of the VCO into a low frequency. In our design, the divided ratio is 20. A high ratio requires compensation of the loop to maintain stability of the loop. A large time constant for the low-pass filter is required. The schematic of the Frequency Divided is shown in Figure 2.18. Figure 2.19 is the schematic of the DFF used in Figure 2.18. Table 2.6 shows the transistors sizes of the DFF.

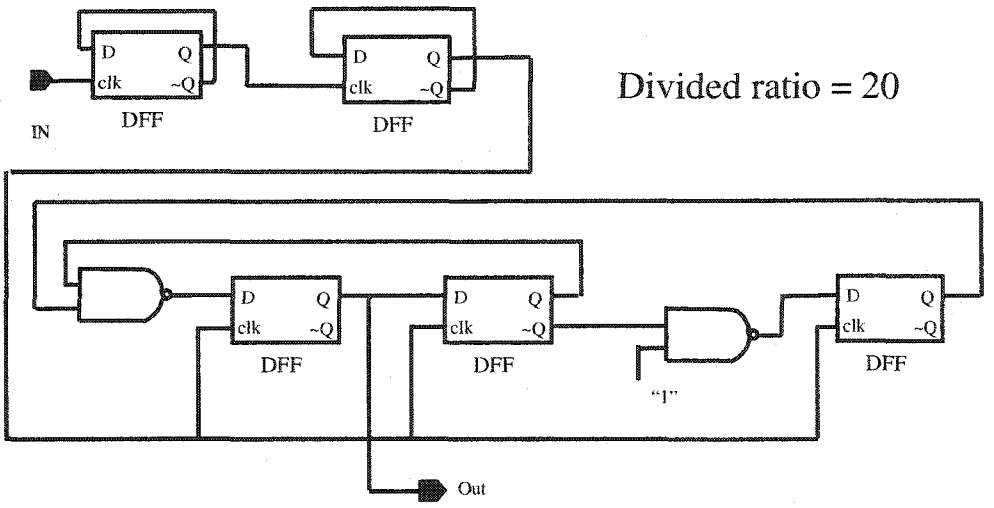


Figure 2.18: Block diagram of the Frequency Divider

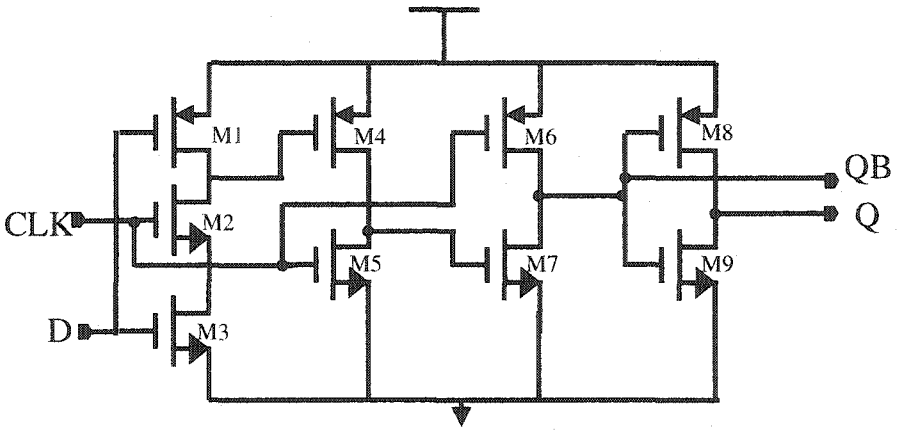


Figure 2.19: Schematic of DFF

Table 2.5: The transistors sizes of the output buffer

W1/L1	W2/L2	W3/L3	W4/L4
6u/250n	6u/250n	6u/250n	6u//250n
W5/L5	W6/L6	W7/L7	W8/L8
3.5u/250n	3.5u/250n	3.5u/250n	3.5u/250n
W9/L9	W10/L10	W11/L11	W12/L12
20u/250n	20u/250n	18u/250n	18u/250n
W13/L13	W14/L14	W15/L15	W16/L16
6.5u/250n	6.5u/250n	12u/250n	12u/250n
W17/L17	W18/L18		
12u//250n	12u/250n		

Table 2.6: The transistors sizes of the DFF

W1/L1	W2/L2	W3/L3	W4/L4
1.76u/250n	1.76u/250n	1.76u /250n	1.76u /250n
W5/L5	W6/L6	W7/L7	W8/L8
2.2u/250n	2.5u/250n	2.5u/250n	5u/250n
W9/L9			
2.52u/250n			

2.3.2.10 Start-up circuitry

A start-up circuit is needed for the PLL. The reason for need of a start-up circuitry will be discussed now. When the power is turned on, the electronic states of the internal nodes in the loop are undefined. Sometimes the voltage of the bias-generator input node will be out of the required operation region. In this case, the bias-generator won't work correctly. Sometimes, the bias-generator works properly but the control voltage is too low. The relationship of the control voltages and oscillating frequency is inversed proportional. So extremely low control voltage will cause a very high output frequency of the VCO. If the bandwidth of the frequency divider is not high enough, the clock information will be lost at the output of frequency divider.

The simple start-up circuit shown in Figure 2.20 was used. A voltage divider formed by two MOS transistor generates a voltage, V_{ref}. The value of V_{ref} should be in the VCO operation range and the accuracy of V_{ref} is not critical. When the power is turned on, switches S1 and S2 are on and the control voltage node is forced to be V_{ref}. Vpulse that turns

on or off S1 and S2 can be got from other digital circuitry on the same chip and generally cost nothing. Figure 2.20 shows the structure of the start-up block.

2.4 Simulation Results

The simulation results are based on TSMC 0.25μm process available through MOSIS program.

2.4.1 The transfer characteristic of slaveVCO

There are two transfer characteristics of the slave VCO. One is the relationship between the output frequency of the slave VCO and the control voltage V_p and V_n (or V_{ctrl}) that come from the PLL loop. The other one is the relationship between the frequency and the control voltage that comes from an external input (V_{x2}). Figure 2.21 shows the first type transfer characteristic of the slave VCO at different process and temperature corners. The results show that the VCO has a large gain to cover the process and temperature variations. On the other hand, Figure 2.22 and Figure 2.23 show the transfer characteristic of the slave VCO in which the control voltage comes from an external input V_{x2}. The former shows the effect of both temperature and process variation and the latter only temperature variation. These results show that the VCO can have a small gain to cover the incoming data variations.

2.4.2 VCO frequency variation due to temperature change

The slave VCO output frequency was simulated when the temperature was swept from 0°C to 100 °C with a step of 20 °C for every fixed control voltage V_{x2}. V_{x2} was swept from 0 to 2.5V. The master VCO was used to generate the voltage V_{ctrl} in this simulation.

Figure 2.24 shows the VCO frequency variation due to temperature change over 0 °C to 100 °C, while the control voltage V_{x2} was varied from 0 to 2.5V. In order to get a clear picture, the curves for V_{x2} equal to or less than 0.9 V are redrawn in Figure 2.25.

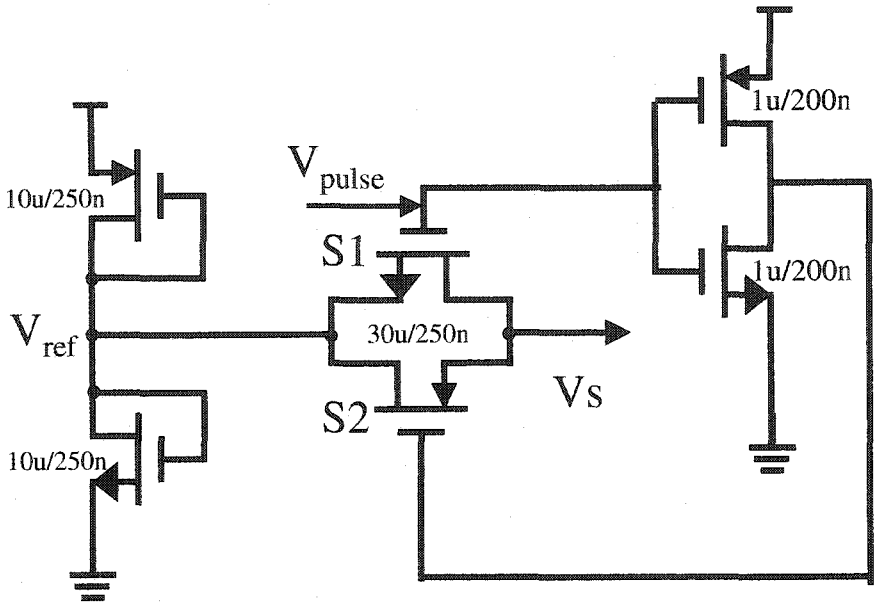


Figure 2.20: The start-up circuitry

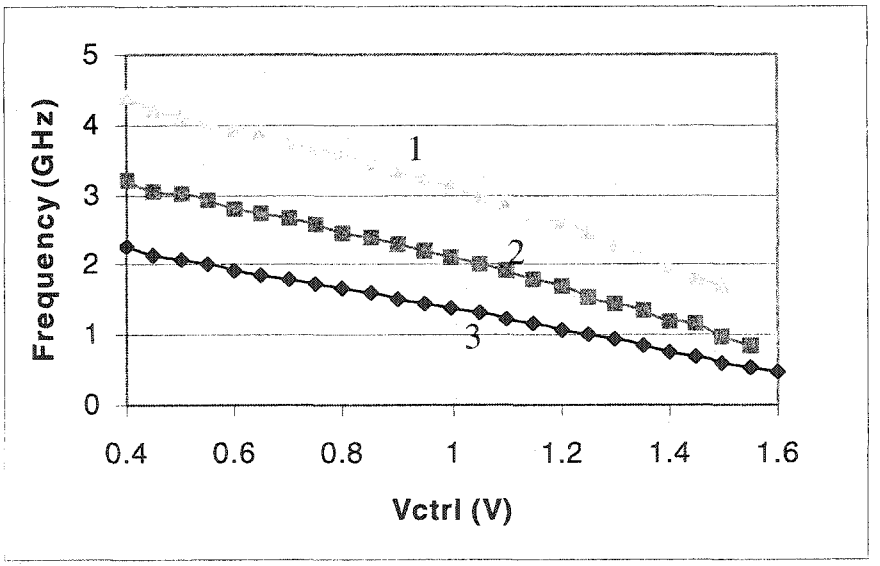


Figure 2.21: The transfer characteristic of slave VCO, the control voltage comes from the PLL. 1) fast process corner, T=0°C; 2) nominal process corner, T=27°C; 3) slow process corner, T=100°C

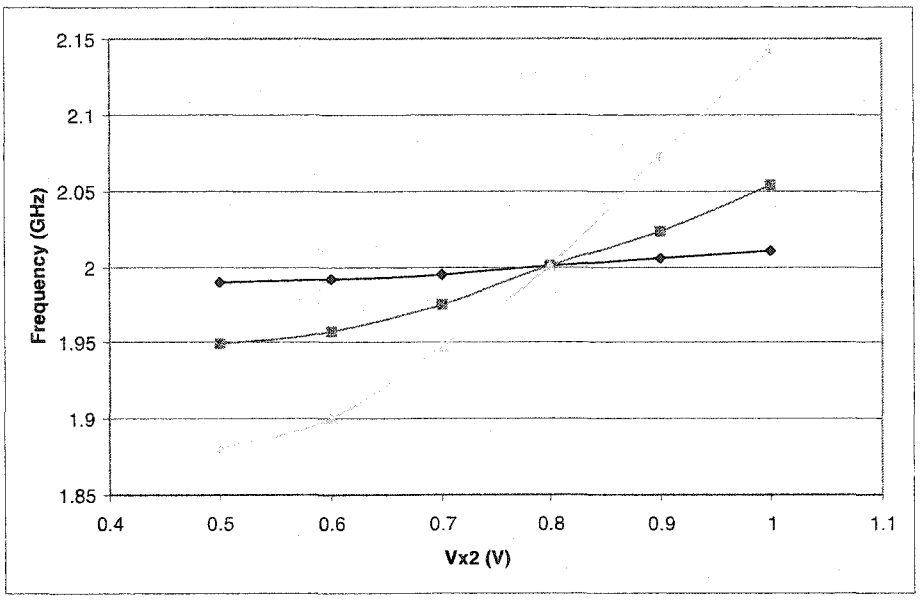


Figure 2.22: Transfer characteristic of the slave VCO, the control voltage comes from the external input V_{x2}. 1) fast process corner, T=0°C; 2) nominal process corner, T=27°C; 3) slow process corner, T=100°C

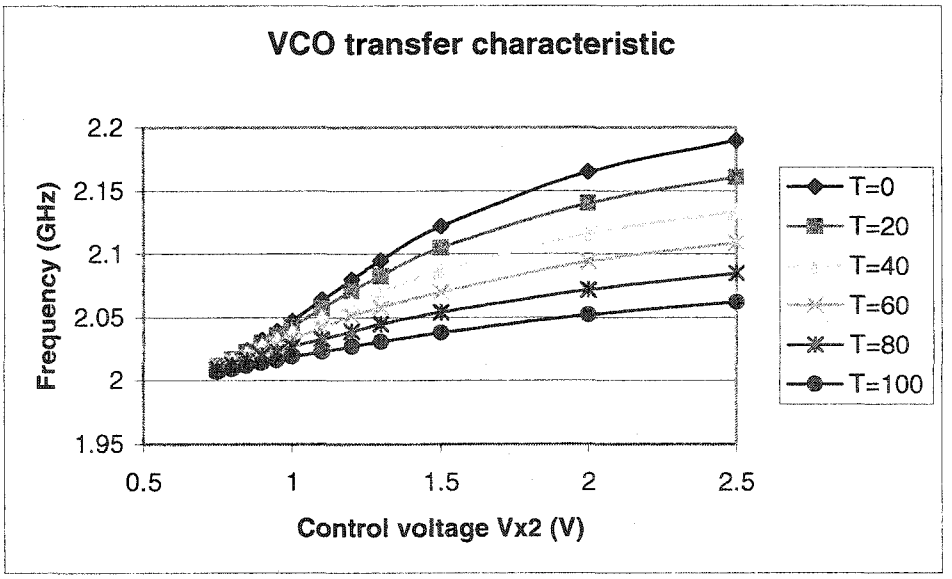


Figure 2.23: Transfer characteristic of the slave VCO over temperature range from 0 °C to 100 °C and at normal process corner, the control voltage comes from the external input V_{x2}.

It can be seen that the frequency variation is 0.5% over the 0 °C to 100 °C temperature range when V_{x2} is 0.85 V. The impact of the temperature on the frequency is more obvious with the increase of V_{x2}, but the frequency variations are still modest even for larger value of V_{x2}. The largest variation is 5.8% over the 0 °C to 100 °C temperature range at the condition that V_{x2} is 2.5 V. Although a relative larger variation was seen when V_{x2} is 2.5 V, it is not of concern because the VCO adjusted range for V_{x2} from 0 V to 0.85 V is enough for the applications that the required frequency variation due to system frequency variation requirement is only 1% of the center frequency. Furthermore, from the results show in the next subsection, a variation of 5.8% is still substantially less than the variation in the circuit without compensation.

2.4.3 Performance improvement with our proposal VCO

Table 2.7 lists the frequency of slave VCO vs. control voltage V_{x2} at best case (fast process corner and low temperature, T=0°C) and worst case (slow process corner and high temperature, T=100°C). It can be seen that the drift of the slave VCO frequency is about ±3.33% over fast and slow process corners and over the 0 °C to 100 °C temperature range. Compared to a ±40% drift for the same VCO without the temperature and process compensation, using the temperature and process compensated VCO enables a reduction in VCO frequency variation of a factor in excess of 10, which will help reduce jitter in clock and data recovery circuits that use the PLL.

Figure 2.26 shows that the VCO without temperature and process compensation has a frequency variation of 10% over the 0 °C to 100 °C temperature range and the slave VCO in our proposal has a frequency variation of 0.5 % over the same temperature range. There is a factor of 20 improvement in frequency drift with proposal VCO.

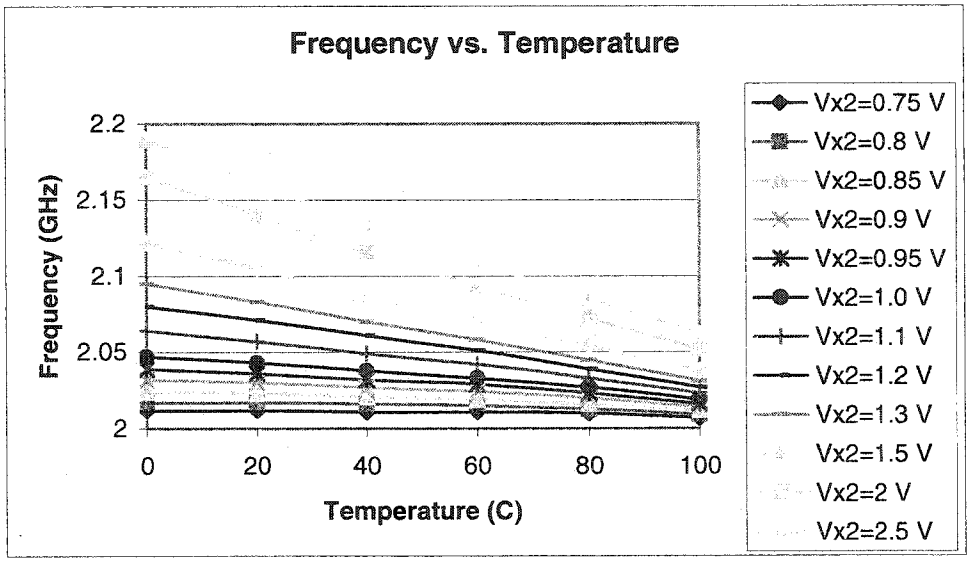


Figure 2.24: Slave VCO frequency variation due to temperature change

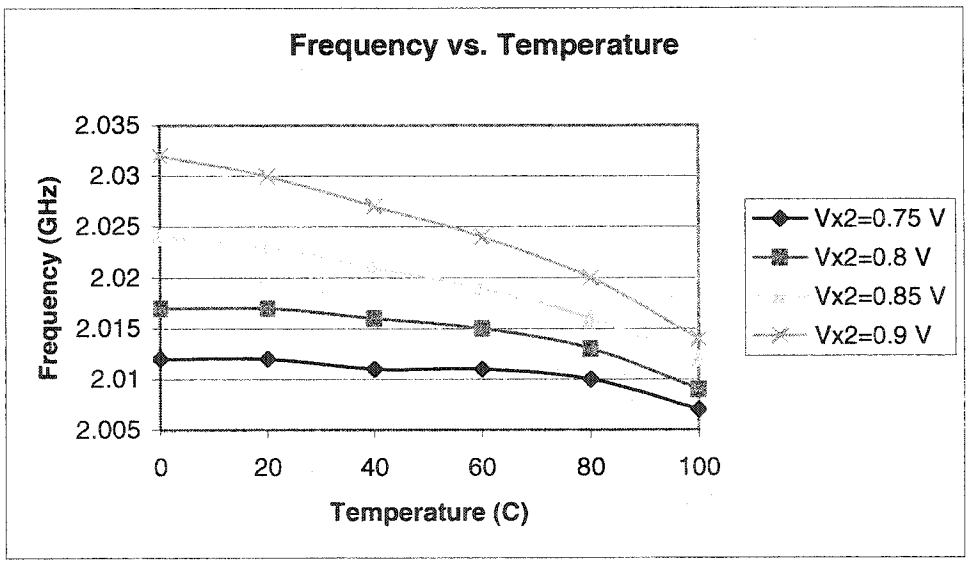


Figure 2.25: Slave VCO frequency variation due to temperature change, maximum variation required on the slave VCO output is at 1% of its center frequency

Table 2.7: Frequency of VCO2 vs. control voltage V_{x2} for best case and worst case.

Control Voltage V_{x2}* (V)	Freq. of VCO2 @ fastest process corner, and T=0 °C (best case) (GHz)**	Freq. of VCO2 @ slowest process corner, and T=100 °C (worse case) (GHz)***	Variation (%)
0.7	1.95	1.995	-2.43
0.8	2.00	2.00	0
0.9	2.07	2.005	3.33

Note:

* This voltage comes from external signal or slave PLL.

**The control voltage from master PLL is 1.44v @ best case

*** The control voltage from master PLL is 0.55v @ worst case

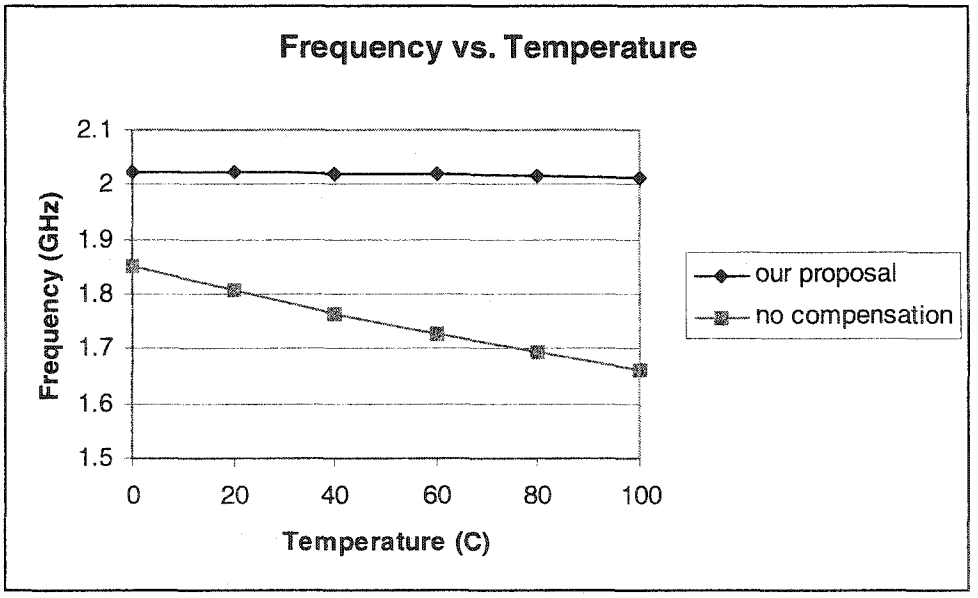


Figure 2.26: Comparison of frequency drift between our proposal VCO and the VCO without compensation

2.5 Chip Fabrication and Test Board Design

In high-speed circuits, a good circuits design is not sufficient to achieve good performance because noise coupling can dramatically degrade circuit performance. The noise coupling can be classified into two categories by considering the means of coupling: circuit coupling between interconnection wires via the parasitic capacitances, resistances and inductances, and circuit coupling between devices via the common substrate body.

To minimize noise coupling, considerable attention was paid to circuit layout, package choice and test board design [21]-[31].

2.5.1 Layout consideration

Analog ICs are more invariable sensitive to noise than digital ICs. For any mixed-signal design with analog circuits and digital circuits on the same chip to be successful, careful attention must be paid to layout design. This includes floorplanning, matching, guard ringing, shielding and other interconnect considerations.

2.5.1.1 Floorplanning

In mixed-signal chips, the floorplanning should be thoroughly considered before the layout is to begin. Figure 2.27 shows a typical mixed-signal floorplan [32]. Low-level signals or high-impedance nodes are considered as sensitive node. These high noise sensitive nodes should be placed far away from or closely guarded and shielded from the noisy digital circuitry. High-level analog signals are less noise sensitive and can be placed between the high noise sensitive analog circuitry and noisy digital circuitry. For the digital signal circuitry, high speed digital output driver will introduce large noise currents to the analog circuits by interconnected lines or the substrate body. These signals with large switch currents should be placed farthest away form the most sensitive analog circuitry. The lower speed digital circuits can be placed between non-sensitive analog circuits and the highest speed digital circuits. Figure 2.28 shows the floorplan of our VCO with the temperature and process compensation circuits. The VCO block contains both VCO1 and VCO2 laid out in a common centroid structure as depicted in Figure 2.29. This circuitry combines both analog and digitals on one chip. In our design, the VCO operation frequency is 2 GHz. The

Frequency Divider operates from 100MHz to 2 GHz, and other digital circuits operate at 100 MHz. The charge-pump and bias-generator are considered as analog circuits and they are physically separated from digital circuits.

2.5.1.2 Matching

Due to variability in the chip fabrication process, parameters of devices will vary as a function of the device size, layout, spaces and orientation [33][34]. In analog and mixed-signal blocks, in order to get good performance, it is often necessary to have accurate matching of the electrical properties of key devices in circuits such as OPAMP, current mirrors, PLLs, etc.

Matching in our case includes two levels of emphasis; one is the transistor level matching in basic components, such as in op amps, Charge Pumps or delay stages. The other is the matching between the delay stages in the VCO. Figure 2.29 and Figure 2.30 show the matching targets in the VCO design.

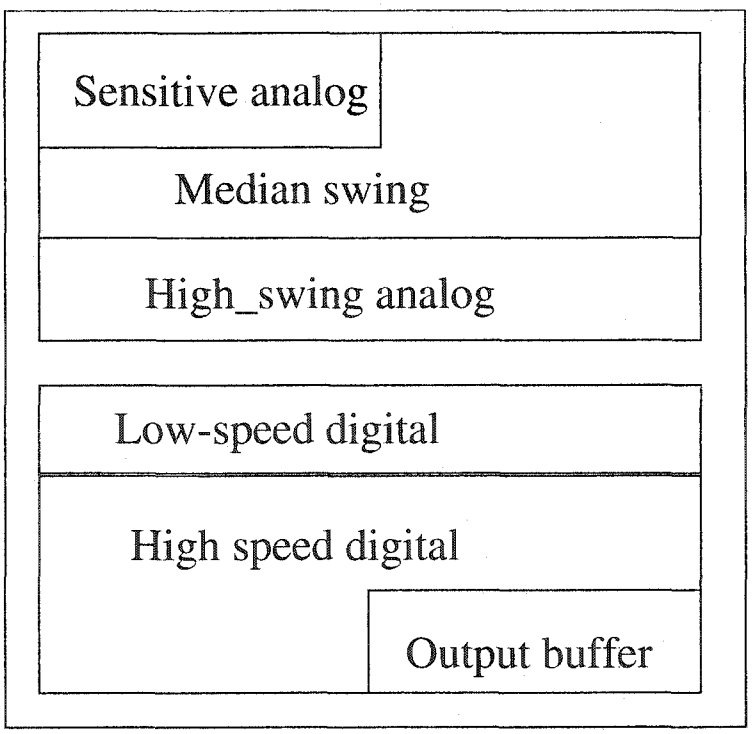


Figure 2.27: A typical mixed-signal floorplan

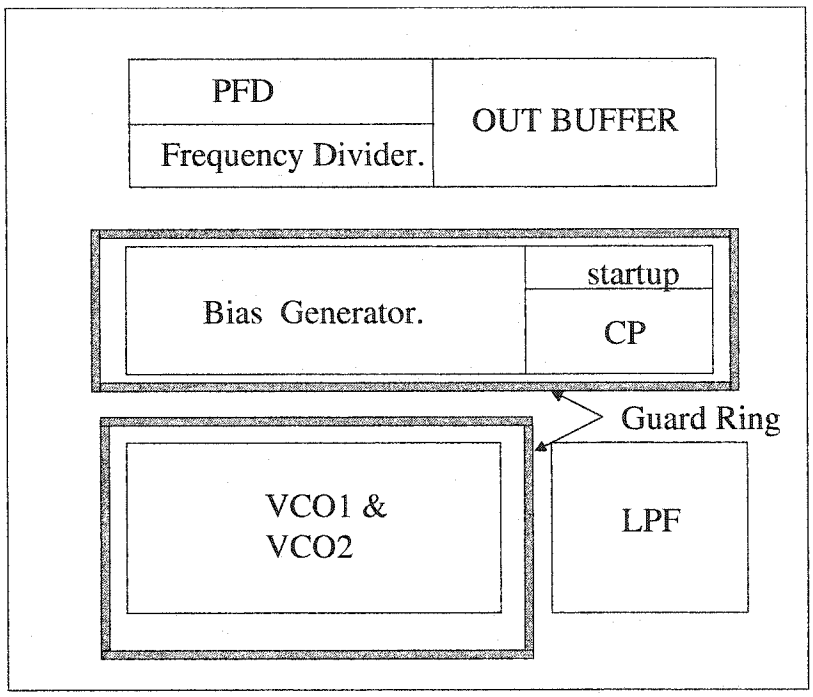


Figure 2.28: The floorplanning of the proposed VCO

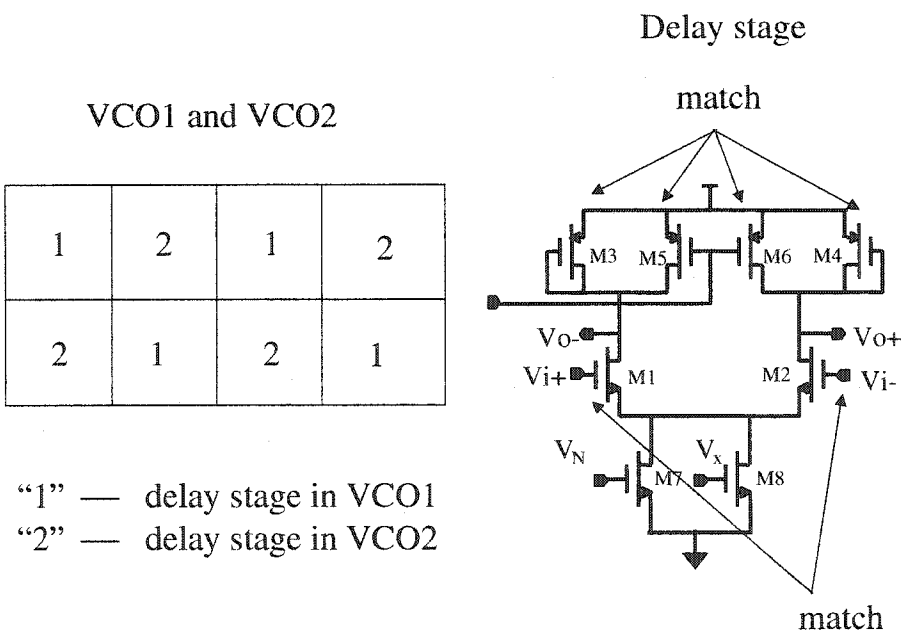


Figure 2.29: Matching requirements for the VCO and for the delay staged in the VCO

2.5.1.3 Guard ring and shielding

Guard rings can be useful in latch-up protection, they also provide isolation between different circuits. In this work, guard rings were created by placing a P+ implant (for p-substrate wafer) between critical circuits and connecting them to the most negative supply. The diffusion reduces injected carriers and holds the substrate, ideally, at a fixed potential. In our VCO design, two guard rings are used. One is used to enclose the eight delay stages of the two VCOs and the other used to enclose the Charge Pump and bias generator.

Shielding is commonly used to reduce the coupling noise from the parasitic capacitances of signal wires. A shield can take the form of a layer tied to analog ground placed between two other layers or it can be a barrier between two signals running in parallel. Figure 2.31 shows two shielding methods that are used in our layout

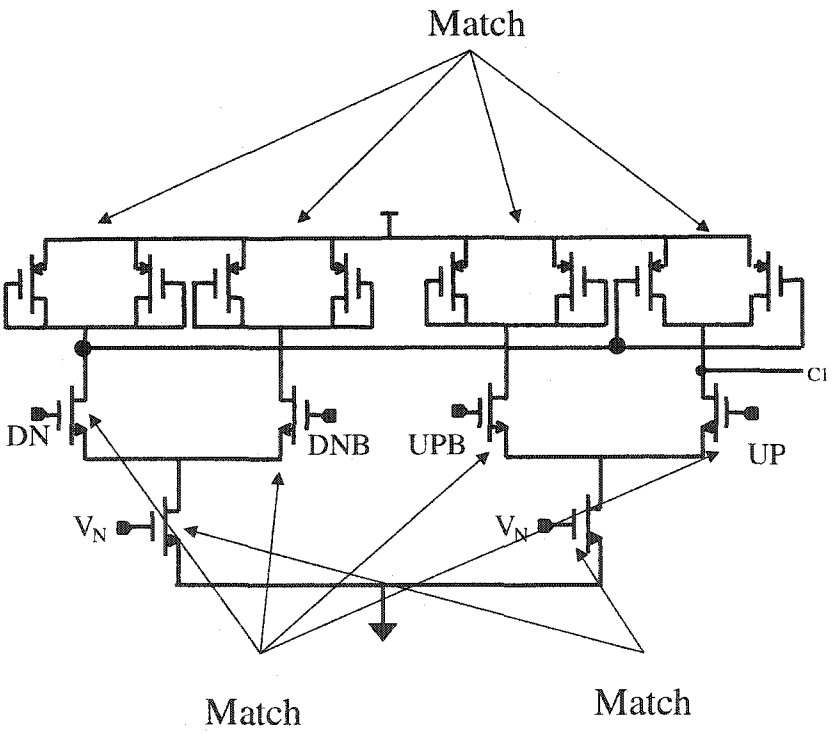


Figure 2.30: Matching requirements in Charge Pump.

2.5.1.4 Power supply and grounding issues

In mixed-signal system, analog circuits and digital circuits reside together on the same substrate. In such system, high amounts of transient current due to switching in digital circuits will result in significant voltage spikes on the power supply and ground rails. Low-level analog signals are very sensitive to such voltage interference. Another significant voltage spike will occur due to the inductance of the bonding wire.

Careful consideration on how power and ground are supplied to both analog circuits and digital circuits is essential to minimize the interference noise through the power supply and ground rails. One way to reduce the interference is to prohibit the analog and digital circuit form sharing the same interconnect and pins. In our VCO design, three sets of pins for power supplies and grounds are employed, one is for digital circuit, one is for the VCO, and one is for bias generator, Charge Pump and other analog circuits.

Another way to reduce the interference is to reduce the parasitic resistance and inductance. Keeping pins closest to the die edge for sensitive connection such as analog supply and ground is a good strategy. The use of double bond wires for supply and ground is also beneficial. Both methods were widely used in our design. Figure 2.32 shows the layout of our design. This layout is done by following the previous floorplan.

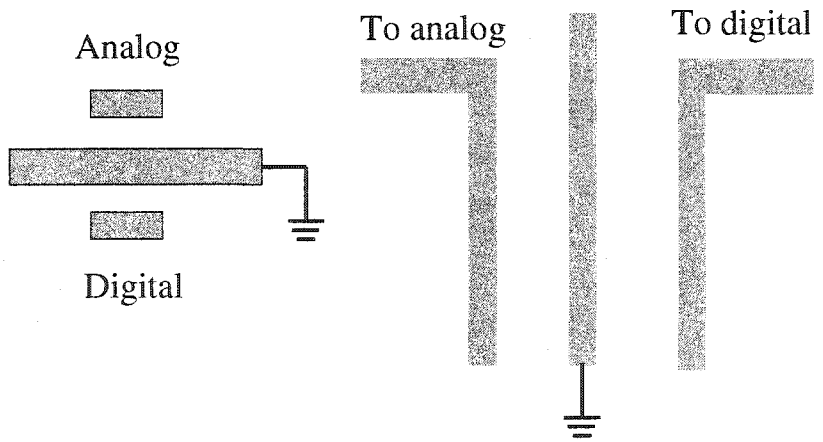


Figure 2.31: Two shielding methods used in our design.

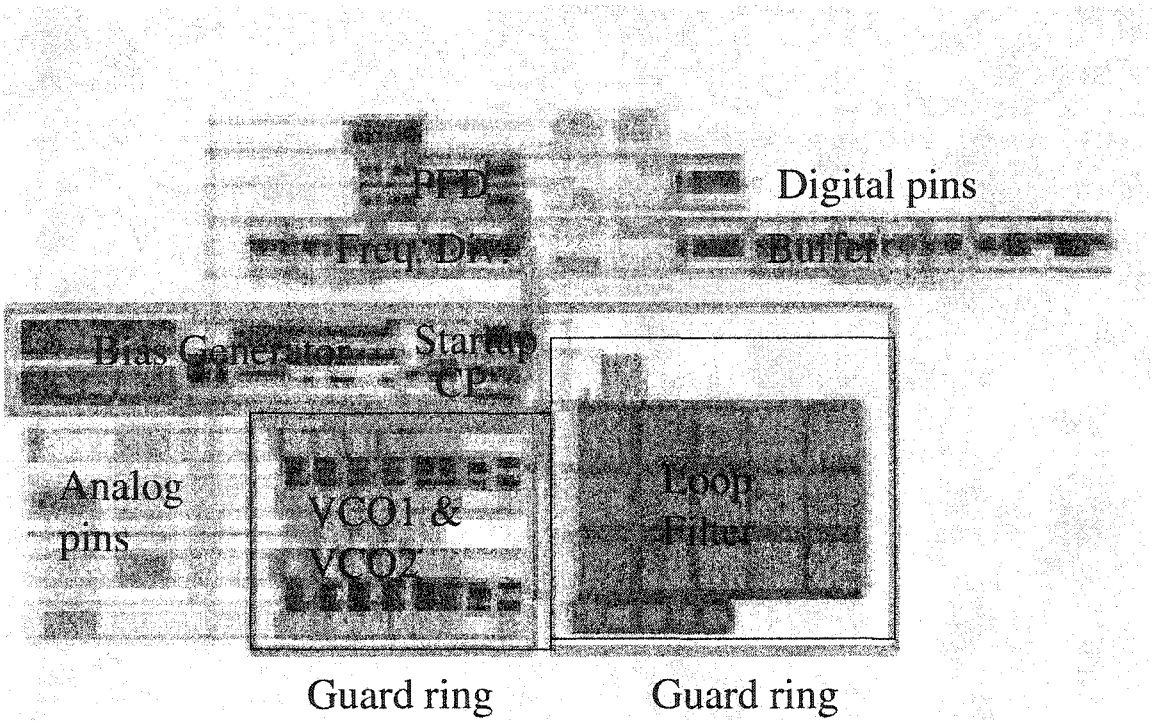


Figure 2.32: Layout of our design

2.5.2 Packaging design

Packaging supplies the chips with signals and power, removes the heat generated by the circuitry, and provides physical support and environmental protection.

In a high-speed circuit, due to large valve of *dI/dt* (ΔI noise), the ground bounce or crosstalk will significantly degrade the performance of the circuit. Traditional through-hole packages such as DIP or PGA are not suitable for high frequency applications. One possible package for our high frequency circuit is a surface mounting device (SMD) such as SOIC, PLLC, LCCC, and PQFP. Surface mounting packages are soldered directly to a circuit board with no intervening leads. This type of die mounting reduces the lead inductance and capacitance a lot. This can be employed in high-speed applications. But the surface mounting package still has a parasitic inductance of 4 nH to 10 nH per pin, it is not small enough for some high-speed applications. The best package is no package at all. That means direct

mounting the chip on the printed circuit board. For our prototype, wire bond was used for making electrical connecting to the die. This "package" dramatically reduced parasitic capacitance and inductance. Figure 2.33 shows the placement of the bonding wires of our prototype.

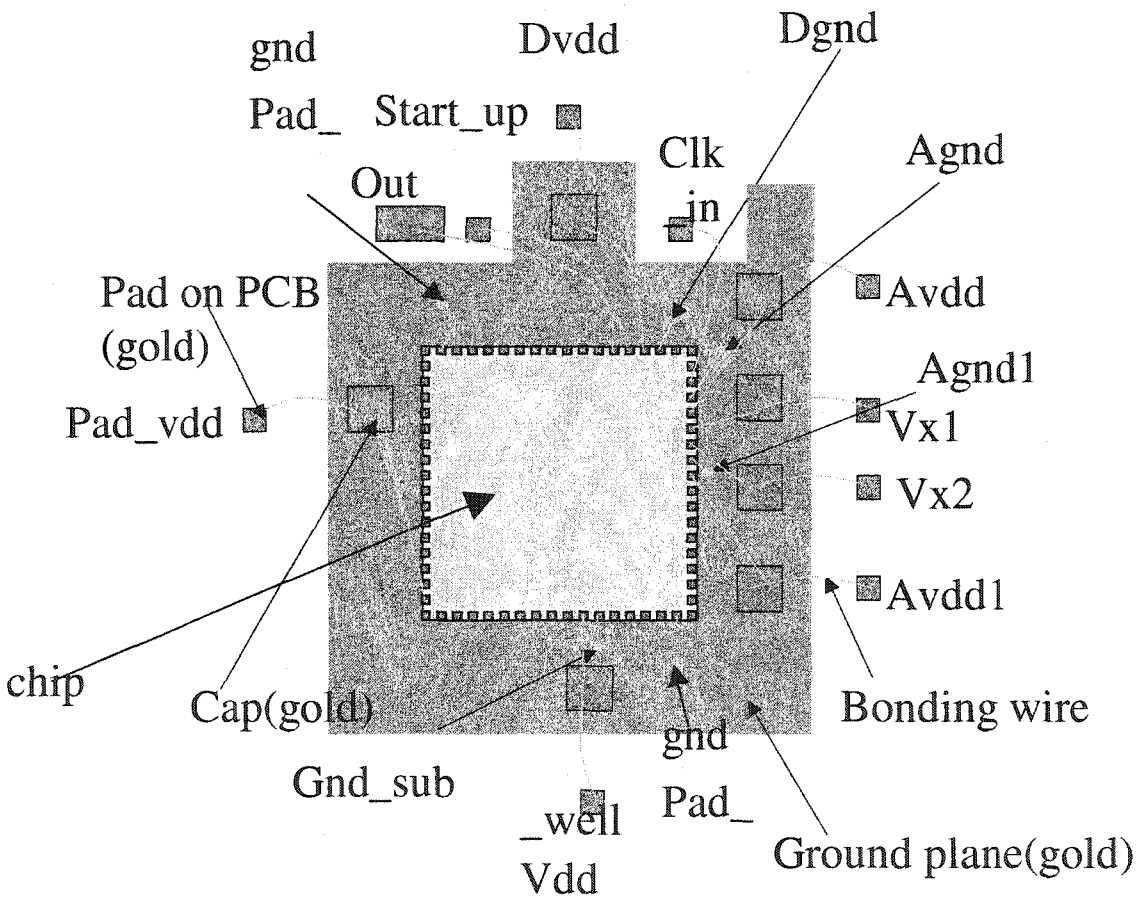


Figure 2.33: Bonding package for VCO with process and temperature compensation

2.5.3 Printed circuit board design

As with the packaging, the printed circuit board design also plays an important role in circuit performance. Poor PCB design can limit parasitic performance or even compromise basic functionality. Key components and approaches to PCB design include bypass capacitor, decoupling capacitor, impedance match and termination.

2.5.3.1 Bypass capacitor

A bypass capacitor is need to create an AC shunt to remove undesired energy from entering susceptible areas on the circuit in addition to providing other functions such as filtering (band-width limiting). It is well known that power supply noise induced by simultaneously switching current from digital circuits will degrade the circuit performance. The distribution of the power supply must be done in a manner providing a low impedance path between the power and ground. Failure to meet this goal at a high frequency will result in voltage spikes when fast switching currents are demanded by the devices. Failure to meet it at low frequencies will result in voltage droop when stable currents are demanded by the devices[35] [36].

Generally, at least one bypass capacitor is needed for every PCB. The capacitance value of the bypass capacitor should be sufficiently large to make the impedance small at the specific frequency of operation. The choice of the bypass capacitor is depend on the tolerance of the voltage drop (ΔV) at the supply wires, the maximum step change in supply current (ΔI), and the lead inductance between the power supply unit (PSU) and the printed circuit board (PCB). As a rule of thumb, bypass capacitors are chosen in the range of 10-470 μF.

2.5.3.2 Decoupling capacitors

Ideally, the distribution of the power supply should present no coupling between devices. Failure to meet this goal will result in spikes or droops produced by one device affecting neighbor devices. Decoupling provides a high frequency, low impedance path to ground for IC switch noise. Decoupling capacitors also serve as a small reservoir for

transient power demands and are particularly useful in reducing peak current surges propagated across the board.[35][36]

Generally, one decoupling capacitor is needed for every IC on the board. Decoupling capacitors usually are placed in parallel with the bypass capacitors. The value of the decoupling capacitor is usually 1/100-1/1000 of the bypass capacitor. As a general role of thumb, the decoupling capacitor is in the value from 4.7n~100nF.

At very high frequencies, the parasitic inductance of on-chip power distribution metals cannot be ignored. On-chip power bus decoupling becomes important in reducing switching noise. For package-level power distribution, the discrete chip capacitors may not be sufficient because their parasitic inductance is not low enough to decouple at very high frequencies[35]. The provision of adequate decoupling capacitance in the power distribution system includes both off-chip and on-chip capacitors. In our design, we used single layer chip capacitors served as decoupling capacitors at the package level. Figure 2.34 shows the usage of the layer capacitors as decoupling capacitors.

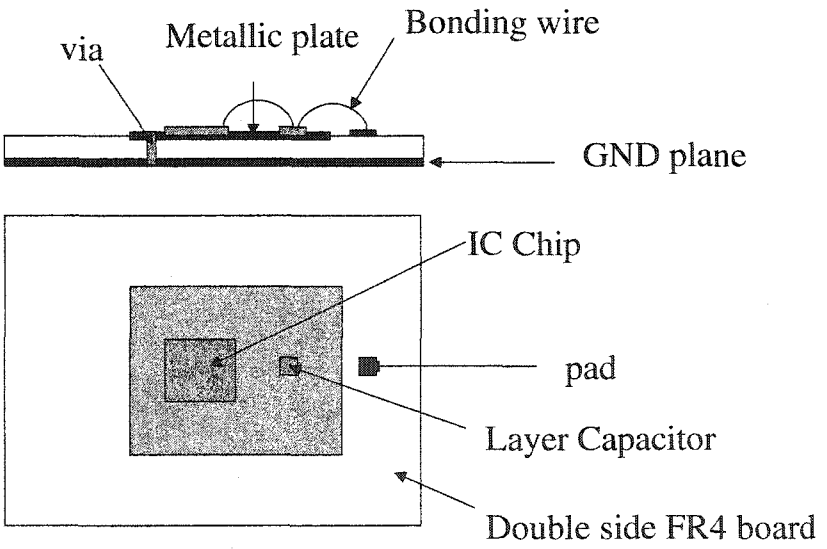


Figure 2.34: The usage of the single layer chip capacitor as decoupling capacitor

2.5.3.3 Impedance matching and termination

For high frequency PCB design, another important issue is impedance matching and termination. A transmission line with a characteristic impedance of Z_o will require resistive termination that matches this line impedance. Transmission of high integrity wideband signals is possible over properly terminated transmission lines. When a signal ground plane is used, the characteristic impedance of a track on the surface (shown in Figure 2.35) is given by Equation (2.22) [37]

$$Z_o = \frac{87}{\sqrt{\varepsilon_{eff}} + 1.41} \ln\left(\frac{5.98h}{0.8w + t}\right) \tag{2.22}$$

where h is the distance between the track and ground plane, w is the track width, t is the copper thickness, and ε_{eff} is the effective relative dielectric of the substrate. For the FR4 substrate, ε_{eff} =5 is commonly used for surface microstrip tracking. For a 0.031" FR4 substrate with 0.5oz copper, 56mil wide track has a characteristic impedance of 50 Ω.

The type of termination will depend on the line impedance and the drivers and receivers connected along the line [37] In our design, parallel resistive termination was used (shown in Figure 2.36). The terminal resistor value was 50 Ω.

The placement of components for the final PC board for my design was shown in Figure 2.37.

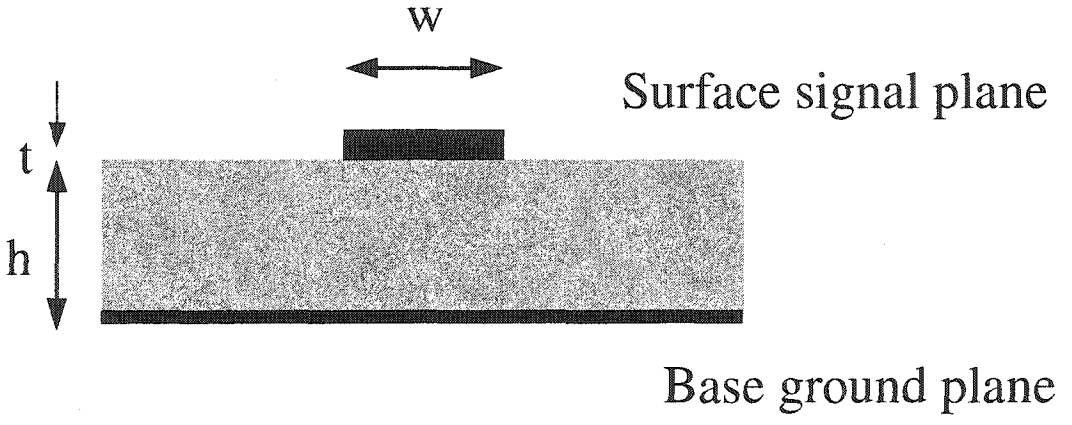


Figure 2.35: Surface microstrip track

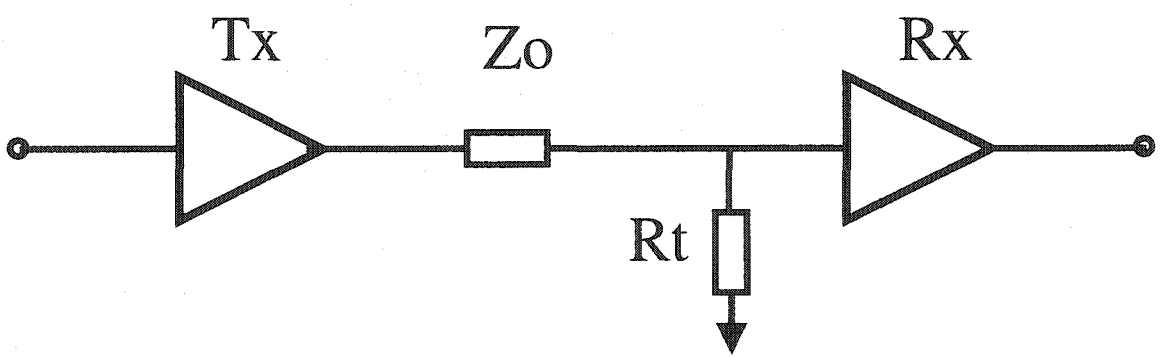


Figure 2.36: Parallel resistive termination

2.6 Test Results

The VCO chip described above was tested in our laboratory. After the chip was fabricated, no VCO frequency variation due to process change could be measured. So, in this dissertation, only the VCO frequency variation due to temperature variation was measured. This may, in part, be due to the small number of test devices available. During the experiment, the whole test board was placed in an oven where temperature can be adjusted from 0 °C to 100 °C. Figure 2.38 shows the measurement set up.

2.6.1 The transfer characteristic of VCO

The transfer characteristic of the VCO was obtained by measuring the slave VCO output frequency when the control voltage V_{x2} was swept from 0 to 2.5V. Figure 2.39 shows the test results of the VCO transfer characteristic. From Figure 2.39, if the maximum variation required on the slave VCO output is at most 1 %, (in our case, from 2 GHz to 2.02 GHz), a change of control voltage V_{x2} from 0 V to 1 V will provide this adjusted range. Figure 2.40 shows a zoomed view of the VCO transfer characteristics. It can be seen that the slave VCO has a VCO gain of approximately 90 MHz/V (This gain is refer to the external inputs V_{x2}). This low VCO gain is very useful for reducing jitter caused by the noise at the control voltage node.

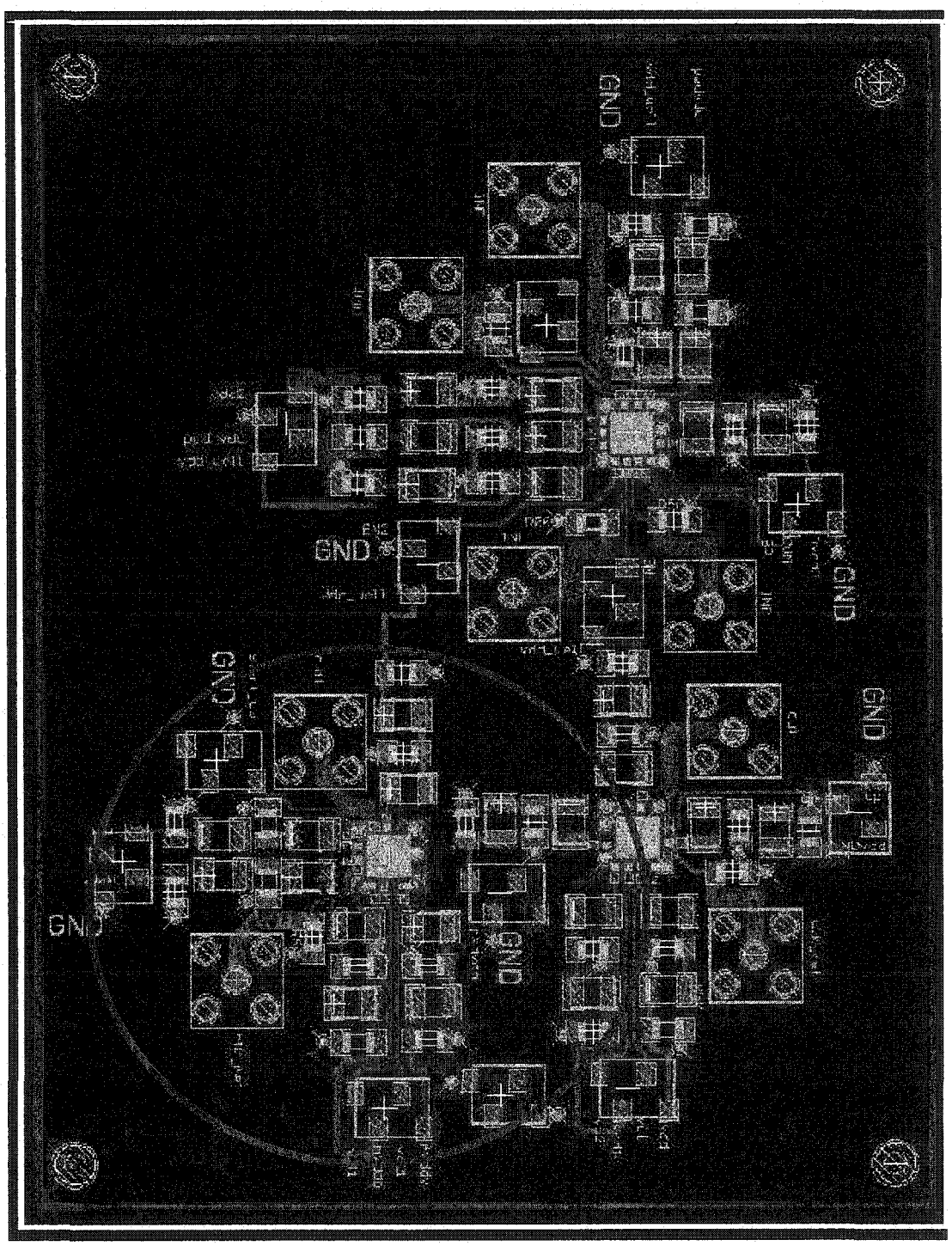


Figure 2.37: Test PCB design, the device inside the circle is the one under test.

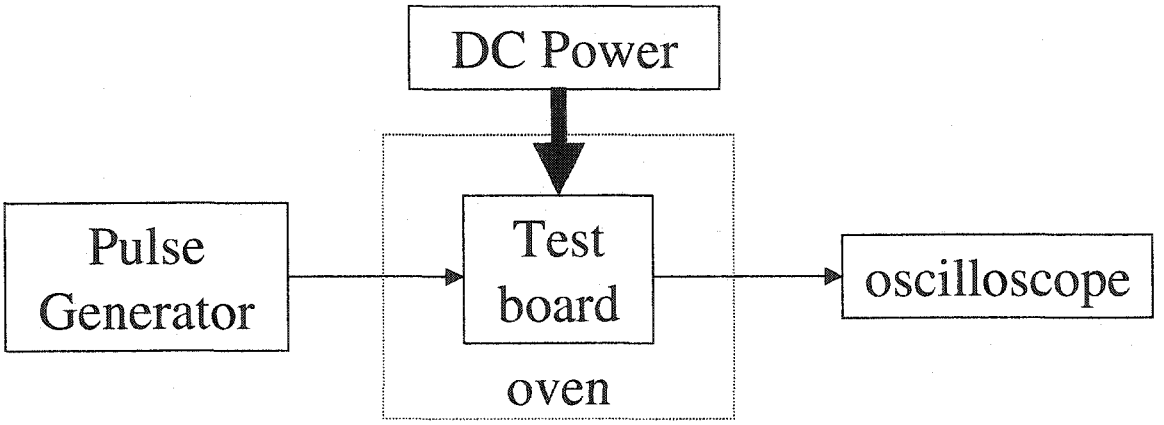


Figure 2.38: The set up for measurement

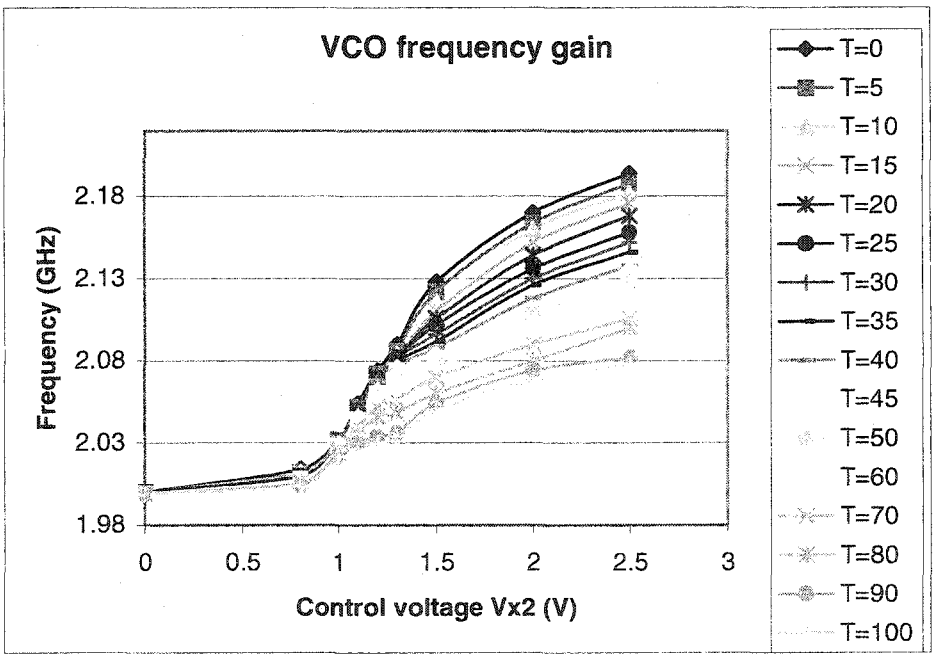


Figure 2.39: Transfer characteristic of slave VCO (freq/V_{x2})

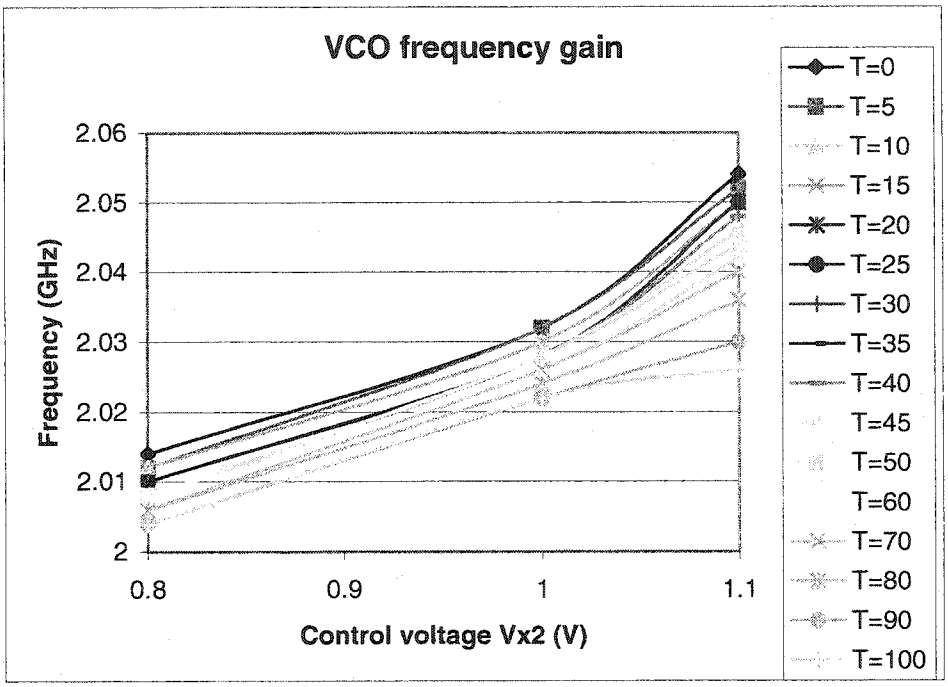


Figure 2.40: Zoomed view of the transfer characteristic of slave VCO (freq/V_{x2})

2.6.2 VCO frequency variation due to temperature change

The slave VCO output frequency was measured when the oven temperature was swept from 0 °C to 100 °C with a step of 10 °C (or 5 °C) for a set of 9 fixed control voltages, V_{x2}, in the range from 0 to 2.5 V.

Figure 2.41 shows the drift of the slave VCO frequency. The curves responding to V_{x2} = 0 V, 0.8 V and 1 V were redrawn in expended view in Figure 2.42. This reflects the desired operating range of the VCO. It can be seen that the frequency variation is at most 1.1% over the 0 °C to 100 °C temperature range, provided that 0 V < V_{x2} <1 V. Thus, for system frequency variation requirements of 1%, the VCO adjusted range for V_{x2} from 0 V to 1 V is more than enough to provide for both temperature compensation and system variation requirements

Although not critical for intended system performance, it can be observed that the variation of frequency with temperature is even modest for larger values of V_{x2}.The largest drift is 5.3% over the 0 °C to 100 °C temperature range and this occurs when V_{x2} is 2.5 V.

The simulation results show the drift of 0.5% at V_{x2}.=0.85V and 5.8% at V_{x2}.=2.5V. It can be seen that the simulation results are very close to the test results for larger values of V_{x2} and have a modest difference for smaller values of V_{x2} .This difference may be due to the CMOS model accuracy at the weak inversion region.

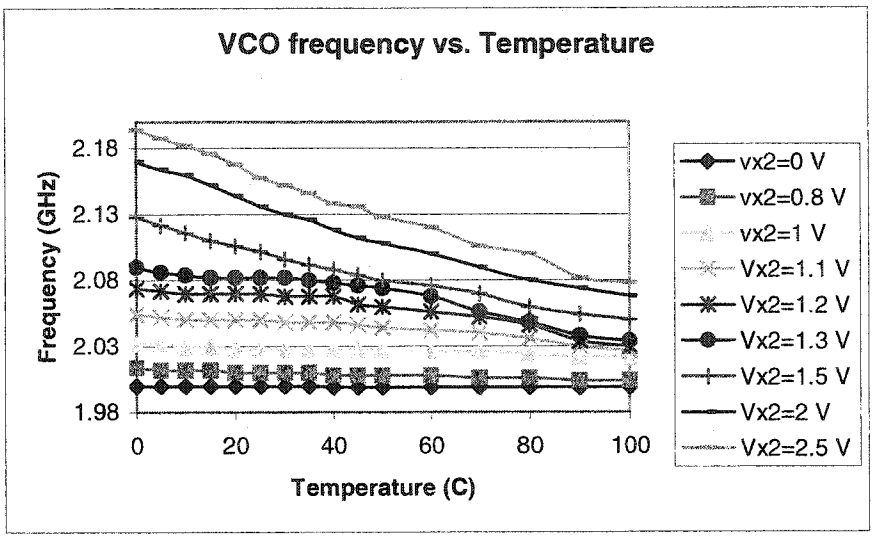


Figure 2.41: Slave VCO frequency variation due to temperature change

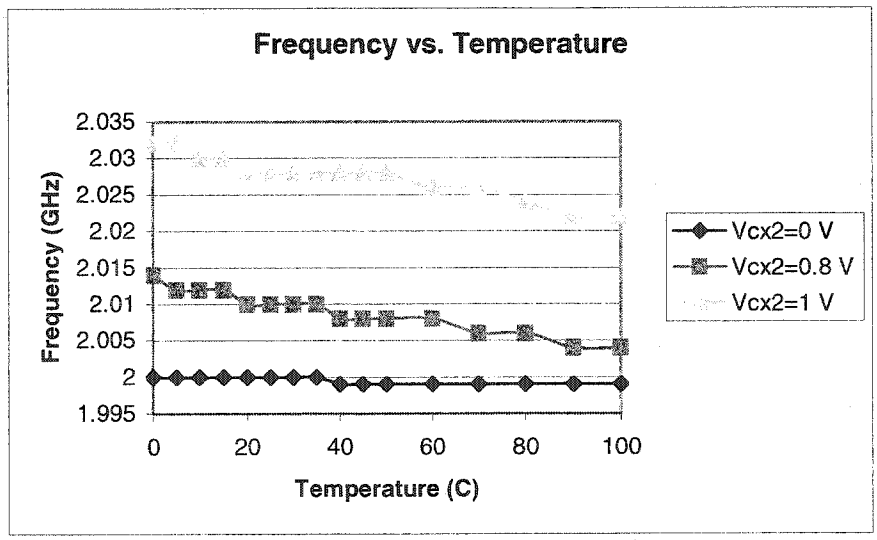


Figure 2.42: Slave VCO frequency variation due to temperature change, maximum variation required on the slave VCO output is at 1%

2.6.3 Performance improvement with our proposal VCO

In order to assess the performance improvement with the proposed VCO, the frequency drift due to temperature variation without compensation was also measured. The block diagram of the VCO is redrawn in Figure 2.43. The temperature compensation network was disabled by setting the reference frequency of the PLL far away from the locking frequency and by adding a fixed control voltage to the Vctrl. Preferably we would have powered down the master VCO and applied a fixed voltage to Vp and Vn of the slave VCO but an oversight in the original design precluded this test in out prototype circuits. However, the test strategy used should adequately break the control loop.

Figure 2.44 shows a comparison of the uncompensated VCO with that of the compensated VCO. The shift in the frequency of the uncompensated VCO is not of concern and is due to the limitation describe above in breaking the loop. It can be seen that the uncompensated VCO has a frequency variation of 11% over the 0 °C to 100 °C temperature range compared to about 1% for the temperature compensated structure. This represents a factor of 10 reduction in frequency drift with the temperature compensated.

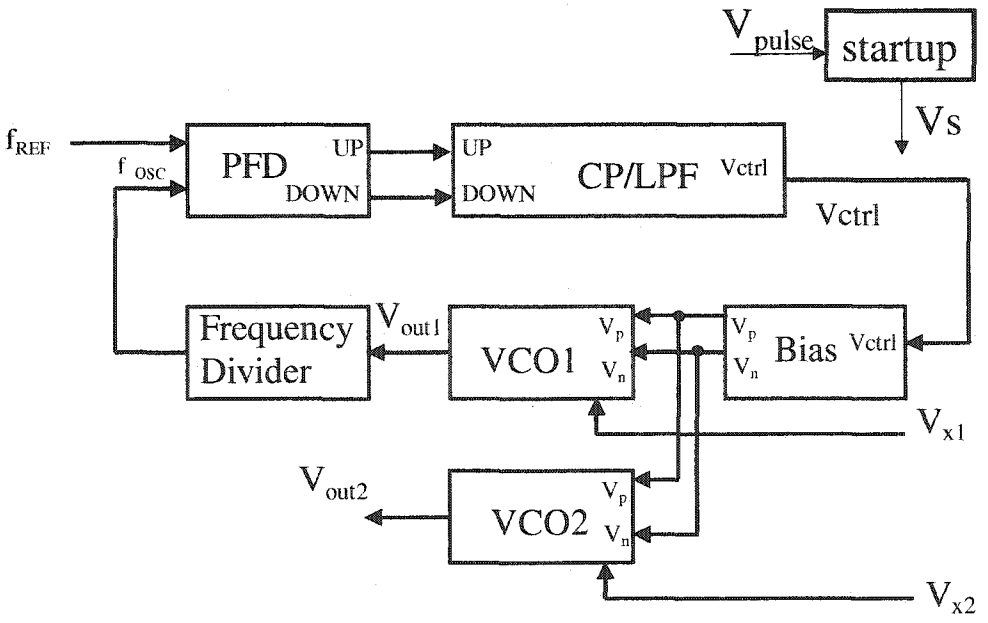


Figure 2.43: Block diagram of temperature and process compensation VCO in 2 GHz implementation

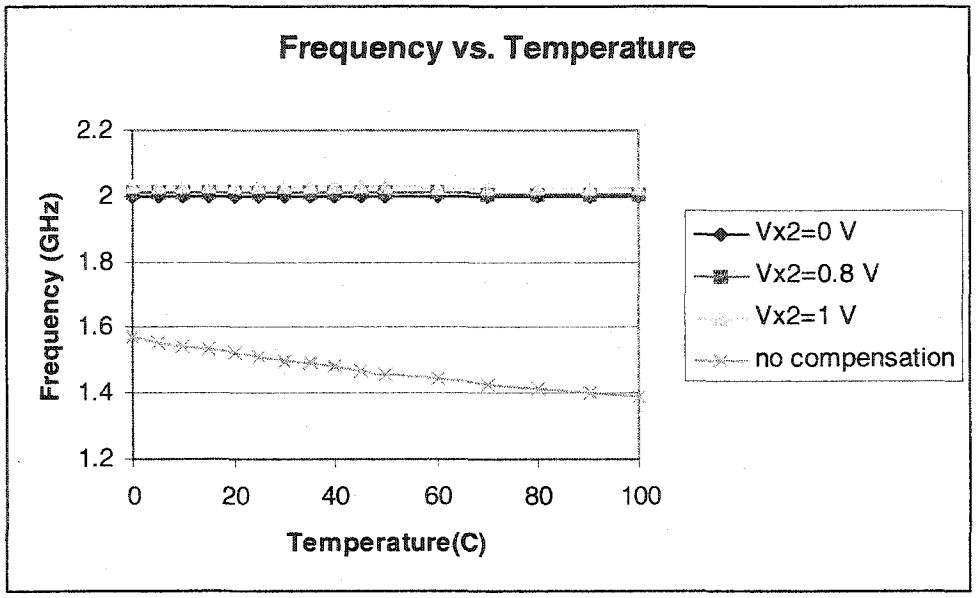


Figure 2.44: Comparison of frequency drift between the proposed VCO and the uncompensated VCO

For uncompensated VCO, both the test results and the simulation results give a frequency variation around 10%. The test results give a factor of 10 reduction in frequency drift with the temperature compensated and the simulation results give a factor of 20 reduction. The reason caused the difference is already addressed in section 2.4.3.

2.7 Conclusions

A temperature and process compensated VCO, which is designed to operate at 2 GHz, and whose frequency variation due to incoming data is limited to 1% of its center frequency was presented. The simulation results show that the circuit has a frequency variation of ±3.33% due to temperature and process changes over fast and slow process corners and over a 0°C to 100 °C temperature range. This is a reduction of in excess of a factor of 10 when compared to a conventional VCO design. If no process changes are presented, simulation results indicated the frequency variation due to temperature change only over the 0°C to 100 °C temperature range is around 0.5% compared to the slave VCO frequency variation associated with system standards that are often bounded by 1% of its

center frequency. This is a reduction of a factor of 20 reduction in temperature sensitivity when compared to the temperature variation of a conventional VCO design. The test results show that, without process changes present, the frequency variation due to a temperature change over 0°C to 100 °C is around 1.1% of its center frequency. This is a reduction of a factor of 10 when compared to the temperature variation of a conventional VCO. A dramatic reduction in the required sensitivity of the VCO frequency to the control voltage is thus possible, specifically a reduction of over a factor of 10. This will result in a significant reduction in jitter in a PLL that uses this VCO in the loop.

CHAPTER 3 PERFORMANCE CHARACTERIZATION OF CMOS VOLTAGE CONTROLLED RING OSCILLATOR

3.1 Problem Definition and Motivation

In Chapter 2, a new design of VCO with process and temperature variation compensation is presented. In this chapter and the next chapter, we will focus on the design of VCO. The more detailed VCO theory and design considerations will be given. The basic delay stage that is used in the previous chapter is redrawn in Figure 3.1. In this delay stage, a differential input structure with the current sources paralleled with diode-connected load is used to reduce the supply and ground noise. Two controlled voltages V_P and V_N provide large operation frequency tuning range. Diode-connected PMOS transistors provide common mode and swing of the output signal.

One of the important properties of any VCO is the transfer characteristic, which is the relationship between the control voltages and the operation frequency of the output signal. Although this delay stage is widely used in the VCO design, the accurate transfer function has not been presented yet. In some applications, it is not required that the VCO has a linear relationship between the operation frequency and the control voltages. But for almost all the applications, the monotonic relationship between the operation frequency and the control voltages is necessary. This chapter will provide a detailed analysis about the transfer characteristic of the VCO. The results show that the transfer characteristic for the VCO is not monotonic, so careful design is suggested to make sure that the VCO operates in the monotonic transfer characteristic region.

3.2 Literature Review

A ring oscillator consists of a number of delay stages in a loop. Figure 3.2 shows the typical block diagram of a ring oscillator. If the delay stage is a single-ended inverter, the total number of inverters in the loop must be odd so the circuit does not latch up. If the delay stage is a differential stage, the total number of the stages may be even.

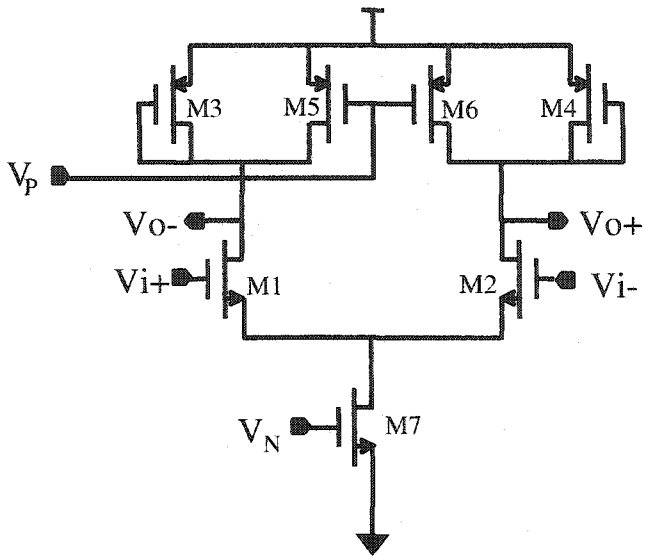


Figure 3.1: Delay cell in Chapter 2

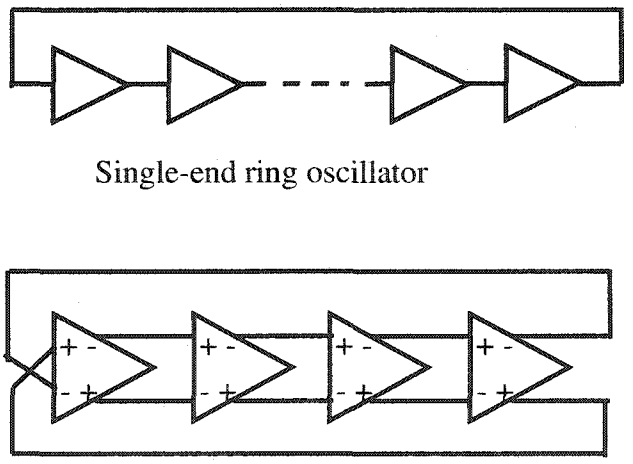


Figure 3.2: The block diagram of a typical ring VCO

There are many ways to implement the delay stages. Figure 3.3 shows some of commonly used delay stages. Figure 3.3a is a single-ended current-starving inverter; it has the simplest structure and provides wide operation frequency turning range. Compared to the differential structure, it has low device jitter [38] [39], but its performance is limited by the

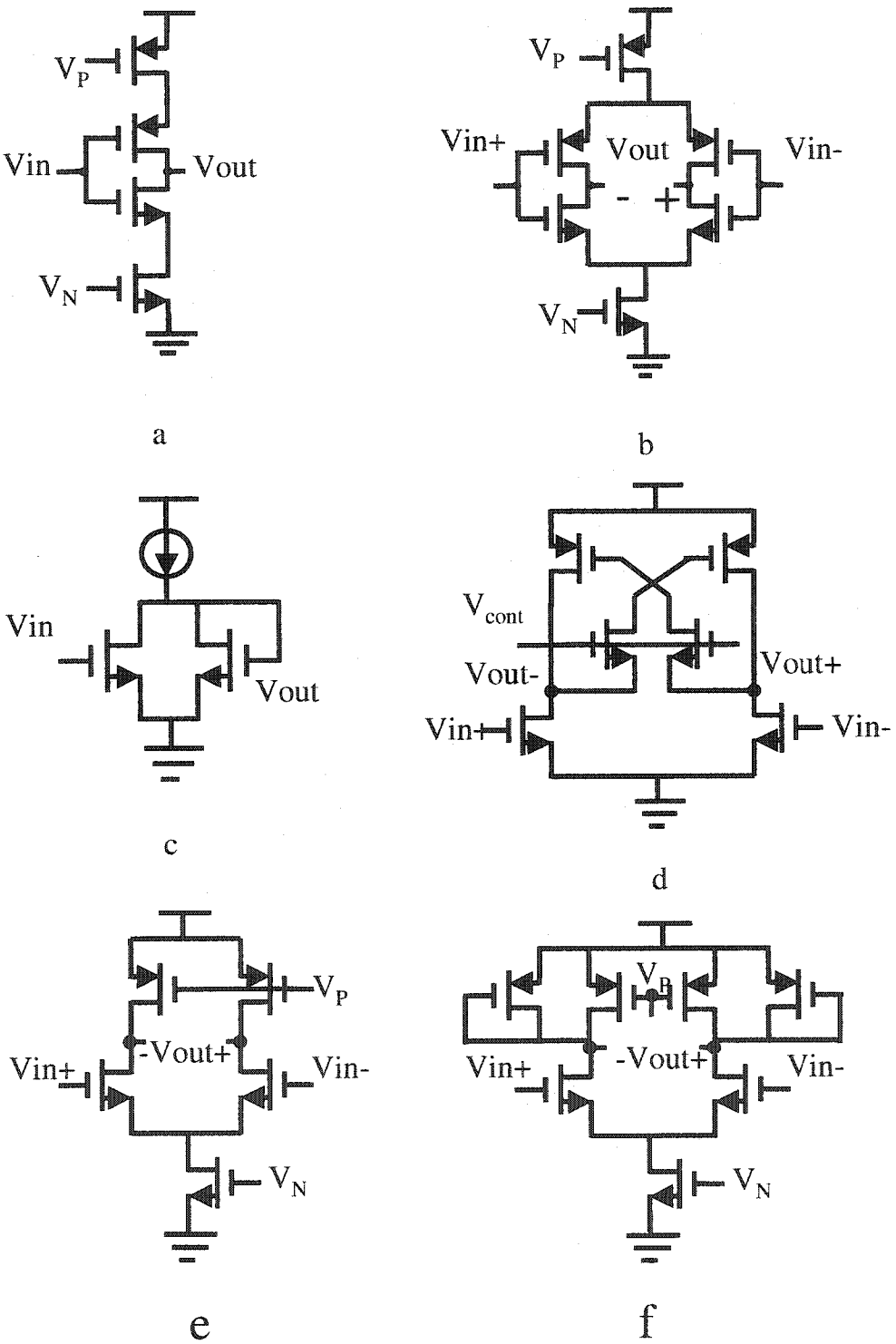


Figure 3.3: Commonly used delay cell in VCO

low supply and ground noise rejection. Figure 3.3b is the differential version of Figure 3.3a. In Figure 3.3b, the supply and ground noise is rejected as the common mode noise. Figure 3.3c has a positive relationship between the output swing and operation frequency, and consequently has a good SNR at high frequency. It also has a good ground noise rejection due to the fact that input and output related to same ground [40]. In Figure 3.3d, Tail current source MOS transistor, which is commonly used in ECL-like differential CMOS pair, is avoided to reduce the 1/f noise. M3 and M4 constitute a CMOS latch. M5 and M6 control the strength of the latch, consequently control the delay. This structure has full swing waveform, consequently less noise and large drive capability. The disadvantage is the reduction of the maximum operation frequency due to M5 and M6 [4]. Figure 3.3e uses differential structure with common source pair inputs and active loads. In Figure 3.3f, PMOS diode M5 and M6 give a fixed common mode and swing of the output voltage. Compared to Figure 3.3e, it has a wide range of operation frequencies and supply voltages. The disadvantage is the reduction of the maximum operation frequencies due to the parasitic capacitance of the diode.

The delay cell shown in Figure 3.3f is widely used in the VCO design. The accurate transfer function has not been presented yet. Some designers thought the operation frequency is directly proportional to the control voltage V_P, while others thought that the operation frequency is reversal proportional to the controlled voltage V_P. In some applications, it is not required that the VCO has a linear relationship between operation frequency and control voltages. But for almost all the applications, the monotonic relationship between the operation frequency and the control voltages is necessary.

3.3 Transfer Characteristic of the CMOS Ring Oscillators

The voltage control ring oscillator is a nonlinear oscillator. The design and analysis of a nonlinear oscillator are complicated tasks, because transform methods (s-plane) cannot be applied directly. Nevertheless, like sinusoidal oscillators, the ring oscillators can be analyzed by two steps. The first step is a linear one, and frequency-domain methods of feedback circuit analysis can be readily employed. Subsequently, a nonlinear mechanism for amplitude control can be provided [41]. The operation frequency of the oscillator is determined in the first step, while the swing of the output signal is determined in the second step.

Figure 3.4 is the behavior model of a ring VCO. Although in an actual oscillator circuit, no input signal will be present, an input signal here is included to help us analyze. Let $A_n(s)$ be the transfer function of one delay stage, $A_f(s)$ be the transfer function of all delay stages, and $\beta(s)$ be the feedback factor. The closed loop transfer function $A_f(s)$ is given by

$$A_f(s) = \frac{A_t(s)}{1 \pm A_t(s)\beta(s)} \tag{3.1}$$

where minus sign is for odd number stages and plus sign is for even number stages. The loop gain of the circuit is defined

$$L(s) \equiv A_t(s)\beta(s) \tag{3.2}$$

The characteristic equation thus becomes

$$1 \pm L(s) = 0 \tag{3.3}$$

According to Barkhausen criterion, at the oscillation frequency ω_0, the phase shift of the loop gain is 2π (for positive feedback) or π (for negative feedback) and the magnitude of the loop gain is unity. Thus the condition for the circuit in Figure 3.4 to provide a stable oscillation at frequency ω_0 is that

$$L(j\omega_0) \equiv A_t(j\omega_0)\beta(j\omega_0) = \pm 1 \tag{3.4}$$

In the ring oscillator case, $\beta = 1$. To satisfy Equation (3.4), we have that

$$A_t(j\omega_0) = |A_t(j\omega_0)| \angle\phi = \pm 1 \tag{3.5}$$

where $\phi = \angle A_t(j\omega_0)$, so that

$$\begin{aligned} &|A_t(j\omega_0)| = 1 \\ &\phi = 2\pi \text{ or } \pi \end{aligned} \tag{3.6}$$

For the delay cell shown in the Figure 3.3f, the transfer function is that

$$A_n(s) = \frac{v_o}{v_i} = -\frac{g_{m1}}{sC + 1/R} \tag{3.7}$$

where g_{m1} is the transconductance of the differential input transistor, C is the total capacitance at the output node of the delay stage, R is the total resistance at the output node, so the total transfer function $A_t(s)$ is that

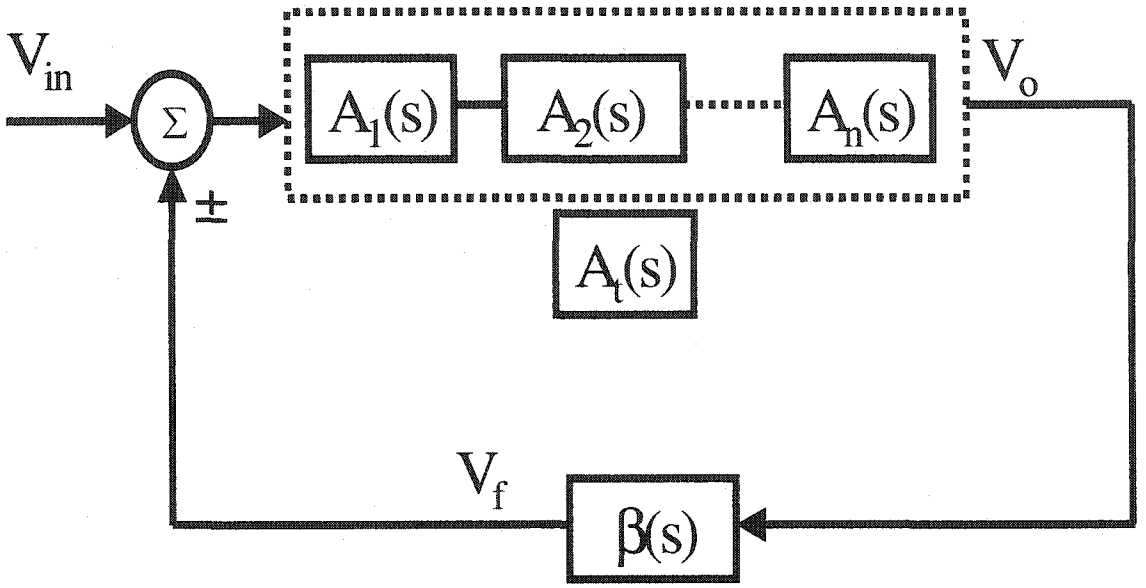


Figure 3.4: The model of a ring oscillator, where plus sign is for odd number stages and minus sign is for even number stages

$$A_t(s) = (A_n(s))^n = \left(-\frac{g_{m1}}{sC + 1/R} \right)^n \tag{3.8}$$

From Equation (3.8), the amplitude and the phase of the transfer function $A_t(s)$ can be expressed as

$$|A_t(j\omega)| = \left(\frac{\frac{g_{m1}}{C}}{\sqrt{\omega^2 + \frac{1}{R^2C^2}}} \right)^n \tag{3.9}$$

$$\phi = n \cdot \tan^{-1}(-\omega RC)$$

At the oscillation frequency ω_0, the amplitude of the gain equals to unity and the phase shift ϕ is 2π, so the VCO operation frequency is

$$\left(\frac{g_{m1}}{C}\right)^n = \left[\sqrt{\omega_0^2 + \left(\frac{1}{RC}\right)^2}\right]^n$$
$$\omega_0 = \frac{1}{RC}\tan\left(\frac{2\pi}{n}\right) \quad or \quad \frac{1}{RC}\tan\left(\frac{\pi}{n}\right) \tag{3.10}$$

Equation (3.10) shows that the operation frequency is determined by the stage number of delay stages in an oscillator, the total capacitance and resistance at the output node of the delay stage. The Equation (3.10) also gives DC gain of the delay stage required for the oscillating, for example n=4, the DC gain of the delay stage equals to $\sqrt{2}$. The total capacitance and resistance at the output nodes depend on the operation region of transistors in a delay stage. These transistors will operate in three regions as the controlled voltage V_P changes. We will analyze the circuit in three cases

Case 1: M5 and M6 are in the saturation region.

Case 2: M5 & M6 are in the triode region.

Case 3: M5 and M6 are in the cutoff region.

3.3.1 Case 1: M5 and M6 are in the saturation region

If all the transistors are in the saturation region, the input and output swing must be less than threshold voltage V_N. So small signal model can be used in the analysis. The small signal model of the half circuit of the delay cell is shown in Figure 3.5, and g_{m1} is given by

$$g_{m1} = \sqrt{\frac{2\mu_n C_{ox} w_1}{l_1} I_1} = \sqrt{\frac{\mu_n C_{ox} w_1}{l_1} I_{tail}} \tag{3.11}$$

Where

$$I_{tail} = \frac{\mu_n C_{ox} w_7}{2 l_7}(V_N - V_{tn})^2 \tag{3.12}$$

Substitute Equation (3.12) into Equation (3.11),

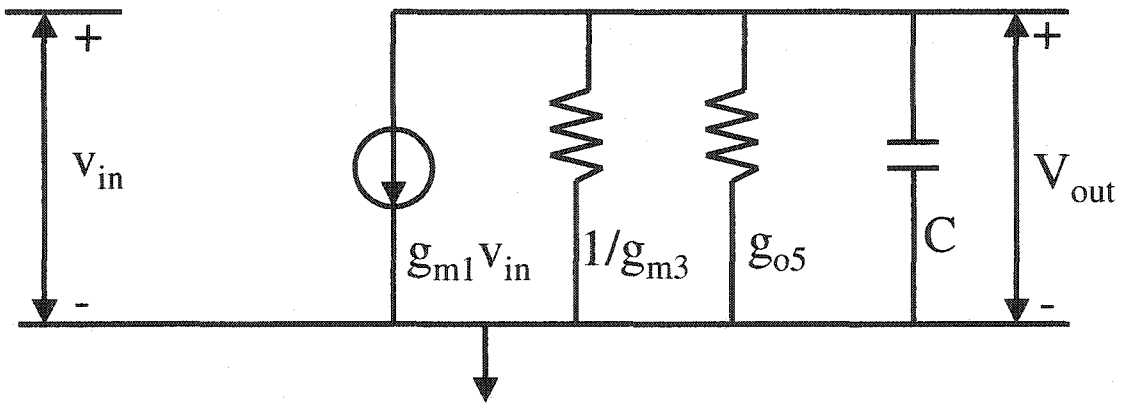


Figure 3.5: Small signal model of delay cell when all transistors operator at saturation region

$$g_{m1} = \sqrt{\frac{\mu_n^2 C_{ox}^2}{2} \cdot \frac{w_1}{l_1} \cdot \frac{w_7}{l_7}} \cdot (V_N - V_{tn}) \tag{3.13}$$

Equation (3.13) shows that g_{m1} is proportional to the control voltage V_N

From Figure 3.5 the resistance and capacitance at the output node are shown in Equation (3.14) and (3.15), respectively.

$$R = (1/g_{o5}) // (1/g_{m3}) \approx 1/g_{m3} \tag{3.14}$$

$$C = C_{gd1} + C_{db1} + C_{gs3} + C_{bs3} + C_{gs5} + C_{bs5} \tag{3.15}$$

Where g_{m3} is the transconductance of M3 and g_{o5} is the conductance of M5.

$$g_{m3} = \sqrt{2\frac{\mu_p C_{ox} w_3}{l_3}(I_{m1} - I_{m5})} = \sqrt{2\frac{\mu_p C_{ox} w_3}{l_3}(\frac{I_{tail}}{2} - I_{m5})} \tag{3.16}$$

Where I_{m1} is the current of M1 and I_{m5} is the current of M5

$$I_{m5} = \frac{\mu_p C_{ox} w_5}{2l_5}(V_P - V_{dd} - |V_{tp}|)^2 \tag{3.17}$$

Substitutes Equation (3.12) and (3.17) into (3.16)

$$g_{m3} = \sqrt{2\frac{\mu_p C_{ox} w_3}{l_3}\left[\frac{\mu_n C_{ox} w_7}{4l_7}(V_N - V_{tn})^2 - \frac{\mu_p C_{ox} w_5}{2l_5}\left(V_P - V_{dd} - |V_{tp}|\right)^2\right]} \tag{3.18}$$

And then substitute Equation (3.18) into (3.14),

$$R = \frac{1}{\sqrt{2\frac{\mu_p C_{ox} w_3}{l_3}\left[\frac{\mu_n C_{ox} w_7}{4l_7}(V_N - V_{tn})^2 - \frac{\mu_p C_{ox} w_5}{2l_5}\left(V_P - V_{dd} - |V_{tp}|\right)^2\right]}} \tag{3.19}$$

Finally substitute Equation (3.19) into (3.10), the operation frequency of the oscillator is

$$\omega_0 = \sqrt{2\frac{\mu_p C_{ox} w_3}{l_3}\left[\frac{\mu_n C_{ox} w_7}{4l_7}(V_N - V_{tn})^2 - \frac{\mu_p C_{ox} w_5}{2l_5}\left(V_P - V_{dd} - |V_{tp}|\right)^2\right]} \cdot \frac{1}{C} \cdot \tan\left(\frac{\pi}{n}\right) \tag{3.20}$$

Equation (3.20) shows that the operation frequency is directly proportional to control voltage V_N and V_P if all the transistors operate in the saturation region.

3.3.2 Case 2: M5 and M6 are in the triode region.

The transconductance of the input transistors g_{m1} is the same as that in case 1, but the total resistance at the output node is different from that in Case 1. Consider the current through M1 (shown in Figure 3.3f) is

$$I = -\frac{\mu_p C_{ox} W_3}{2L_3} \cdot \left[(V_o - V_{dd}) - |V_{tp}|\right]^2 - \frac{\mu_p C_{ox} W_5}{L_5} \cdot \left[\left(V_P - V_{dd} - |V_{tp}|\right)(V_o - V_{dd}) - \frac{1}{2}(V_o - V_{dd})^2\right] \tag{3.21}$$

So the small signal impedance r is

$$\frac{1}{r} = \frac{\partial I}{\partial V_o} = \frac{\mu_p C_{ox} W_3}{L_3}\left[V_{dd} - V_o + |V_{tp}|\right] + \frac{\mu_p C_{ox} W_5}{L_5}\left[\left(V_{dd} - V_P + |V_{tp}|\right) - (V_{dd} - V_o)\right] \tag{3.22}$$

Let $W_3 = x \cdot W_5$ & $L_3 = L_5$

$$\frac{1}{r}=\frac{\mu_p C_{ox} W_5}{L_5}\left[\left(V_{dd}-V_P+\left|V_{tp}\right|\right)+(x-1)(V_{dd}-V_o)+(x+1)\cdot\left|V_{tp}\right|\right] \tag{3.23}$$

Substitutes equation (3.23) into (3.10), the operation frequency of the oscillator is

$$\omega_o=\frac{1}{RC}\tan(\frac{2\pi}{n})=\frac{1}{C}\cdot\tan(\frac{2\pi}{n})\cdot\frac{\mu_p C_{ox} W_5}{L_5}\left[\left(V_{dd}-V_P+\left|V_{tp}\right|\right)+(x-1)(V_{dd}-V_o)+(x+1)\cdot\left|V_{tp}\right|\right] \tag{3.24}$$

Based on the x value, there are three situations:

1. x=1, i.e., the active load is a symmetric load,

$$f_o=\frac{1}{RC}\tan(\frac{2\pi}{n})=\frac{1}{C}\cdot\tan(\frac{2\pi}{n})\cdot\frac{\mu C_{ox} W_5}{L_5}\left[\left(V_{dd}-V_P+\left|V_{tp}\right|\right)+(x+1)\cdot\left|V_{tp}\right|\right] \tag{3.25}$$

The frequency is reversal proportional to the control voltage V_P.

2. x<1, i.e. the size of the diode connect transistor M3 is smaller than that of the PMOS current source transistor M5

Because that V_{dd}-V_o is increased as V_P is increased, so the frequency is also reversal proportional to the control voltage V_P.

3. x>1, i.e. the size of the diode connect transistor M3 is larger than that of the PMOS current source transistor M5.

As V_P is increased, the first term in equation (3.24) is decreased, but the second term is increased, so the relationship of the frequency and the control voltage is undetermined.

3.3.3 Case3: M5 and M6 are in the cutoff region

In this case, equation (3.16) can be rewritten as

$$g_{m3}=\sqrt{2\frac{\mu_p C_{ox} w_3}{l_3} I_{tail}} \tag{3.26}$$

Substitute Equation (3.12) into Equation (3.26), than

$$g_{m3}=\sqrt{2\frac{\mu_p C_{ox} w_3}{l_3}\frac{\mu_n C_{ox} w_7}{2l_7}(V_N-V_{tn})^2} \tag{3.27}$$

The operation frequency of the VCO is given by

$$\omega_0 = \sqrt{2\frac{\mu_p C_{ox} w_3}{l_3}\left[\frac{\mu_n C_{ox} w_7}{2l_7}(V_N - V_m)^2\right]} \cdot \frac{1}{C} \cdot \tan\left(\frac{2\pi}{n}\right) \qquad (3.28)$$

where n is the stage number of the VCO.

Equation (3.28) shows that the frequency of VCO is independent on the V_P

3.4 Simulation Results

The analysis conclusions are verified by using Hspice simulator. The simulation results are based on 0.35 μm CMOS process.

Figure 3.6 shows the relationship of the operation frequency of the VCO and the control voltage V_p. The simulation results show that, if the size of M5 and M6 is larger or equal to that of M3 and M4, the whole voltage controlled range can be divided into three parts. In part I, the transistors M5 and M6 are in the triode region, and the operation frequency is reversal proportional to the controlled Voltage V_P. In part II, M5 and M6 are in the saturation region, and the operation frequency is directly proportional to V_P. In part III, M5 and M6 are in the cutoff region, and frequency is independent on the V_P. If the size of M5 and M6 is smaller than that of M3 and M4, the operation frequency will be directly proportional to control voltage V_P in the whole control voltage range. So in order to make the VCO have a monotonic relationship of the frequency and controlled voltage V_P, careful design is required.

Figure 3.7 shows the relationship of the operation frequency of the VCO and the control voltage V_P and V_N. This result shows that the operation frequency of the VCO is positive proportional to control voltage V_N. By Combining controlled voltage V_N and V_P, the VCO operation frequency tuning range will be from 1.1 GHz to 2.5 GHz at normal temperature and typical process.

3.5 Conclusions

Transfer characterization of VCO is studied in detail. Although most designers believe that the relationship of the frequency and the control voltage is a monotonic relationship, we find, in most situations, the relationship is based on the design sizes and the operation region of the transistors. The Hspice simulation results verified the analysis results.

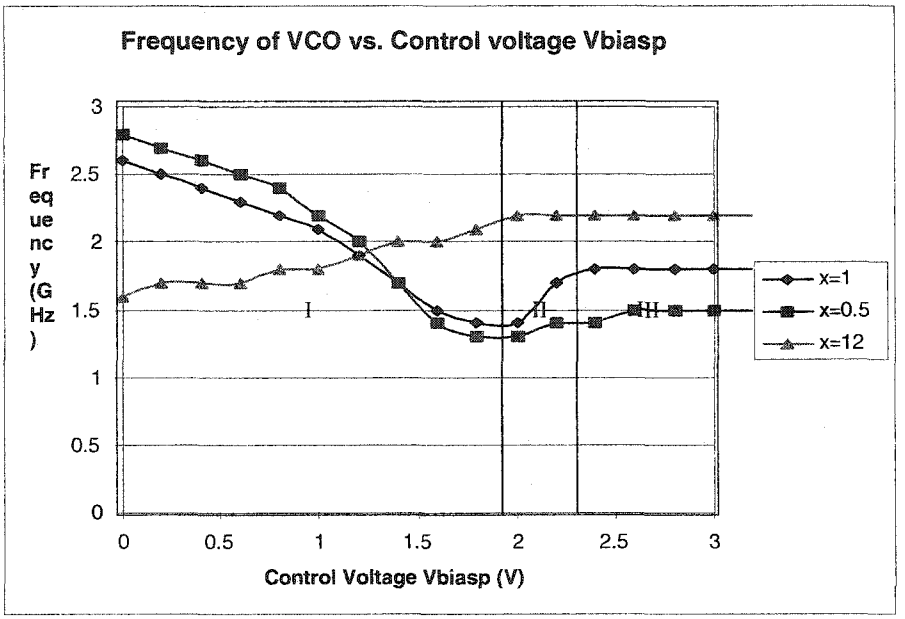


Figure 3.6: Frequency of VCO vs. control voltage V_P. where $x=W_3/W_5$. The operation region of the PMOS current source is in I: triode, II: saturation, and III: cutoff.

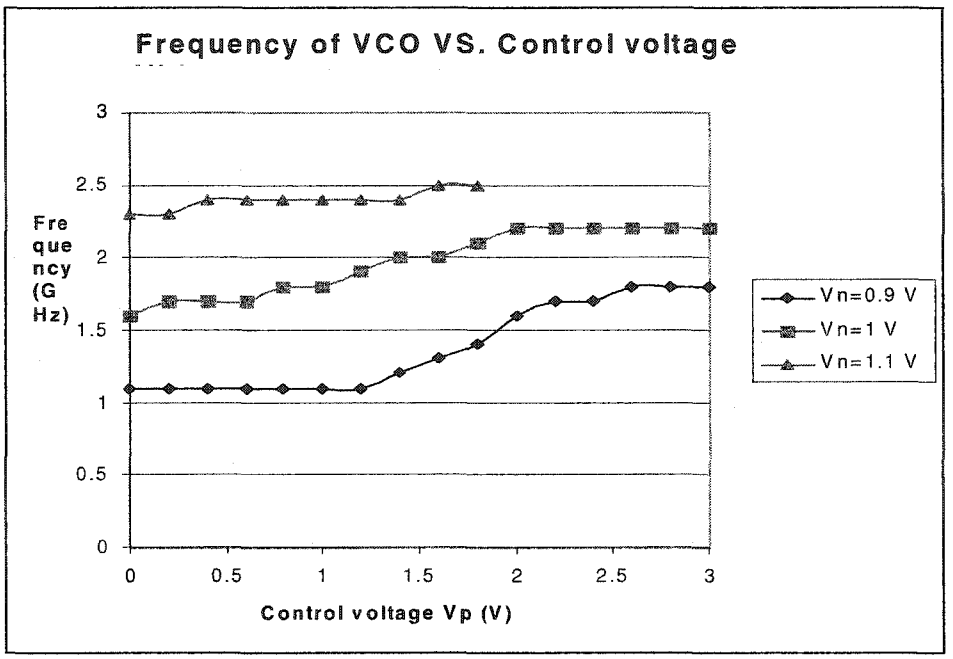


Figure 3.7: Transfer Characterization of VCO (x=12)

CHAPTER 4 MAXIMUM THE VCO OSCILLATION FREQUENCY

4.1 Problem Definition and Motivation

In recent years, there has been a growing interest in very high-speed communication circuits. The design of monolithic VCOs in standard CMOS processes has been the subject of several research efforts. Voltage controlled ring oscillators have relative good jitter performance, large tuning range, monolithic solution, and are low cost. They are widely used in the high-speed communication circuits. Most existing strategies for design of VCOs have been directed at applications where the frequency of oscillation is well below the f_t of a process. In this chapter, we will focus on the impact of layout, load selection and stage gain on high frequency operation.

4.2 Literature Review

There are two commonly used Voltage Controlled Oscillators which have frequencies in GHz range, LC tank oscillators and ring oscillators. In CMOS techniques, the LC tank oscillators are the ones that can reach highest frequency. The reported highest LC oscillator operation frequency in CMOS process is 50 GHz [42]. Other LC oscillators with operation frequency at GHz are often reported recently [43] [44]. However, LC oscillators have some disadvantages. For example, small tuning range, no high quality on-chip inductor, and large chip area occupied make the LC tank unattractive in some applications. On the contrary, ring oscillators can be easily integrated on-chip without any extra processing steps. More important in the industries, ring oscillators normally occupy less chip area, which improves both the yield and the cost. Typically, the operating frequency of the voltage controlled ring oscillators is slower than the LC oscillators. The recently reported highest frequency is 2.8 GHz in 0.35 μm CMOS process [45].

4.3 VCO Design Theory

One common structure for the delay cell of a ring oscillator is shown in Figure 4.1. In this structure, the delay of the cell is a function of the transconductance per unit capacitance of the input transistors and the active loads.

In order to maximize the operating frequency, the output swing of VCO is usually kept small. In such situations, the VCO frequency can be obtained by using a small signal model. Figure 4.2 is the simplified small signal model of the delay cell. In Figure 4.2, g_{m1} and g_{m3} are the transconductance of the input transistors and the load transistors, respectively, and C is the total capacitance seen by the output node. The capacitance C is the sum of the diffusion capacitance on the drain of M1, M3, the load capacitance C_L, and the gate capacitance of the next stage which is essentially $C_{ox}W_1L_1$ where W_1 and L_1 are the width and length of M_1.

The transfer function of the delay stage, assuming loading by an identical stage is:

$$A(s) = \frac{Vo}{Vi} = \frac{-g_{m1}}{sC + g_{m3}} \qquad (4.1)$$

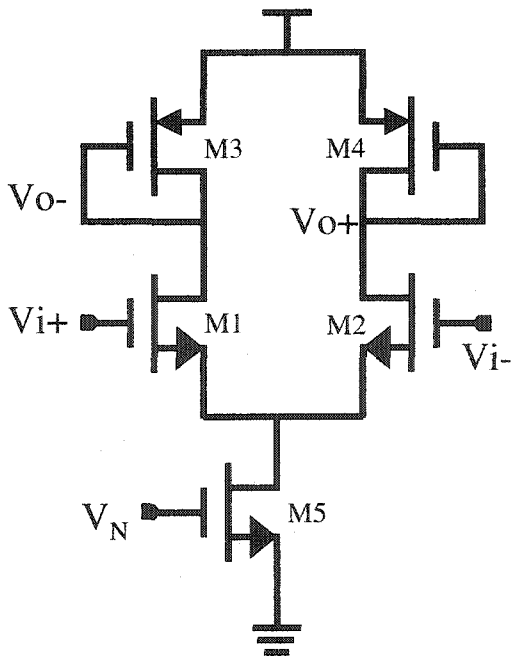


Figure 4.1: Delay cell of the ring oscillator

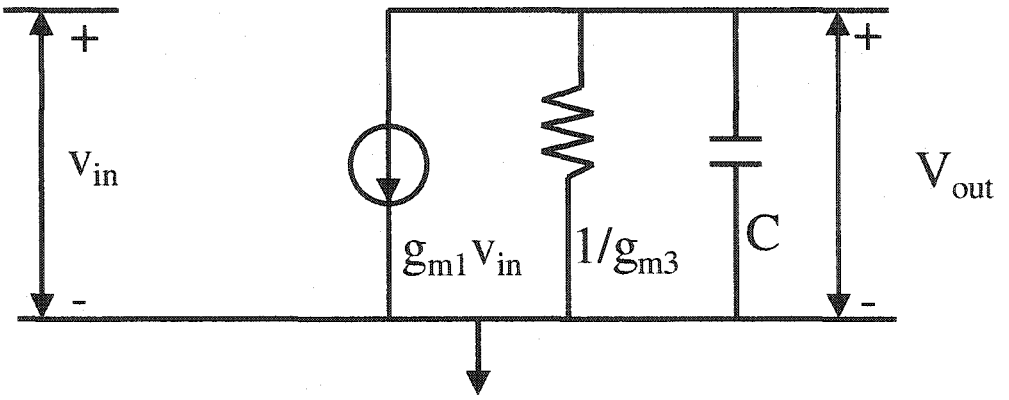


Figure 4.2: The small signal model of VCO delay cell

Since ideally every stage has the same transfer function described by Equation (4.1), the characteristic polynomial of the closed loop of an n stage VCO is

$$D(s) = (s + g_{m3}/C)^n + (-g_{m1}/C)^n \tag{4.2}$$

From (4.2) it follows that the pole locations are:

$$\begin{aligned} p &= (-1)^{\frac{1}{n}} * \frac{g_{m1}}{C} - \frac{g_{m3}}{C} \\ &= \pm\cos(\pi/n) * \frac{g_{m1}}{C} - \frac{g_{m3}}{C} \pm j * \sin(\pi/n) * \frac{g_{m1}}{C} \\ &= \alpha + j * \beta \end{aligned} \tag{4.3}$$

where α is the damping factor of the loop and β is the natural frequency of the loop.

At the onset of oscillation, at least one pair of poles must be located in the right half plane (RHP). The poles move towards the left half plane (LHP) as the loss increases. It can be shown that the output waveform is a pure sinusoid when right-most pair of poles is located on the $j\omega$ axis. In this structure, the damp factor of the loop α, becomes zero. From (4.3) it follows that

$$\cos(\pi/n) * \frac{g_{m1}}{C} = \frac{g_{m3}}{C} \tag{4.4}$$

To sustain oscillation, the pole must be kept on the $j\omega$ axis.

Figure 4.3 shows the pole locations of the VCO under the condition that g_{m3} is established to maintain the damping factor of the right-most pole pair at zero. Under this condition the oscillation frequency of the VCO is

$$\omega = \beta = sin(\ \pi / n\ ) * \frac{g_{m1}}{C} \tag{4.5}$$

Substituting (4.4) into (4.5), the frequency of the VCO can alternately be written as

$$\omega = \cot an(\pi / n) * \frac{g_{m3}}{C} \tag{4.6}$$

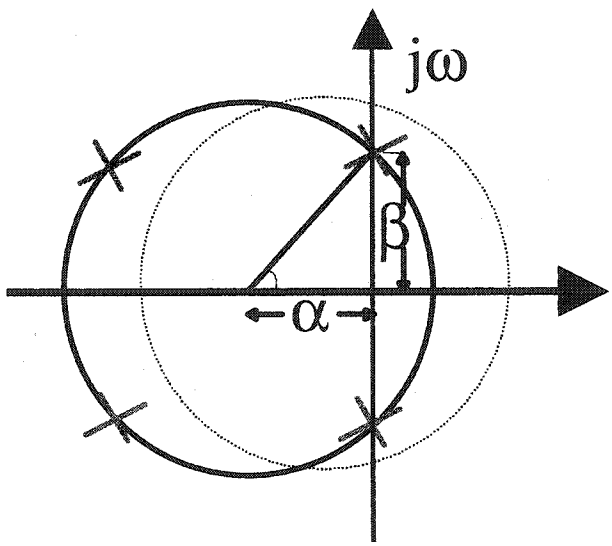


Figure 4.3: The pole location of a 4-stage VCO.

In Equation (4.5) and (4.6), g_{m1} is the transconductance of the input transistor M1. g_{m1} is proportional to the square root of the bias current of the input transistor. g_{m3} is the transconductance of the load transistor M3. g_{m3} is proportional to the square root of the bias current of the load transistor.

From (4.5) and (4.6), the strategy for the design of a high speed VCO is apparent. These can be summarized:

- Minimize the total capacitance seen by the output node.
- Maximize the transconductance per unit capacitance (gm/c) for the input transistors and load transistors.
- Minimize the stage number n.

4.4 High Speed VCO Design Techniques

Most existing strategies for design of VCOs have been directed at applications where the frequency of oscillation is well below the f_t of a process. At higher frequencies, some luxuries afforded the designer tend to limit the oscillation frequency potential of a process. In this section, we will focus on the impact of layout, load selection and stage gain on high frequency operation.

4.4.1 Method 1: Layout techniques for frequency enhancing

The total capacitance seen at the output node and the transconductance per unit capacitance are dependent upon both the process parameters of a given process and the layout of the delay stage. Although layout is not critical for low speed oscillations, it plays an important role in the design of VCOs that are designed to operate at frequencies that approach the f_t of a process. In this subsection, the effect of layout on the frequencies of operation is discussed.

From Equation (4.5) and (4.6), it is apparent that one efficient way to increase the VCO frequency is to minimize the capacitance seen by the output node. This will be minimized when only parasitic and required loading capacitance of the following stage are included. The size of this capacitance is highly layout dependent.

Consider the conventional layout structure shown in Figure 4.4. Following the design rule in a typical CMOS process, the minimum diffusion area of the source and the drain are:

$$A = Drain\ Area = Source\ Area = W*(5\lambda) \tag{4.7}$$

where λ is a scale factor associated with the process that is typically half of the minimum allowable drawn gate length and W is the drawn width of the transistors. Correspondingly, the drain periphery and source periphery are given by

$$P = W + 5\lambda*2 \tag{4.8}$$

In the submicron process, the diffusion capacitance typically dominants the total node capacitance C in a ring oscillator. Thus minimizing the drain or source area will help to increase the VCO operating frequency.

For the conventional layout of Figure 4.4, it follows that the total capacitance C seen on the output node is given by

$$C = C_{ox} W_1 L_1 + C_{sw}(P_1 + P_3) + C_{BOT}(A_{D1} + A_{D3}) \qquad (4.9)$$

where C_{ox} is the gate oxide capacitance density, W_1 and L_1 define the channel geometry of M_1, P_1 and P_3 are the periphery of the drains of M_1 and M_3 respectively, A_{D1} and A_{D3} are the drain areas, and where C_{SW} and C_{BOT} are the sidewall and bottom capacitance densities respectively.

In our research, an alternative layout technique is presented. Figure 4.5 shows the concentric parallel cell layout. It is assumed that every transistor can be divided into k parallel cells, where k is an integer greater than or equal to 1. For every cell, the width and length are approximately 32λ and 2λ, respectively. Assuming the capacitance sensitive node is the drain and the drain is at the inside of the cell. It follows that the area and periphery of the drain and source are given respectively by

$$A_D = 36\lambda^2$$
$$P_D = 24\lambda$$
$$A_S = 300\lambda^2$$
$$P_S = 40\lambda \qquad (4.10)$$

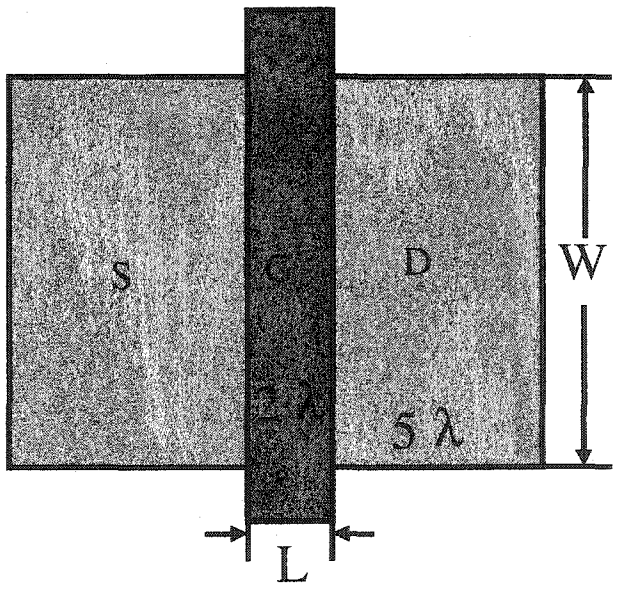


Figure 4.4: Conventional layout structure

Let us examine a simple example. Consider a transistor with a width of 64λ, and a length of 2λ. If the conventional layout structure is used, its drain area is $320\lambda^2$, and the periphery is 74λ. If the concentric parallel cell layout is used, the drain area is only $72\lambda^2$ and the drain periphery is 48λ. If used in a VCO, this reduction in diffusion capacitance will cause the VCO operating frequency increase substantially.

Table 4.1 compares the VCO frequency for a conventional layout and the concentric layout for a 0.35 μm CMOS provided through the MOSIS service by Hewlett Packet. In this table, we selected W_1=150λ, L_1=2λ and k for the load device from 2 to 6.

Form the simulation results, we can see that the improvement of the VCO frequency is about 23% by using the concentric layout technique.

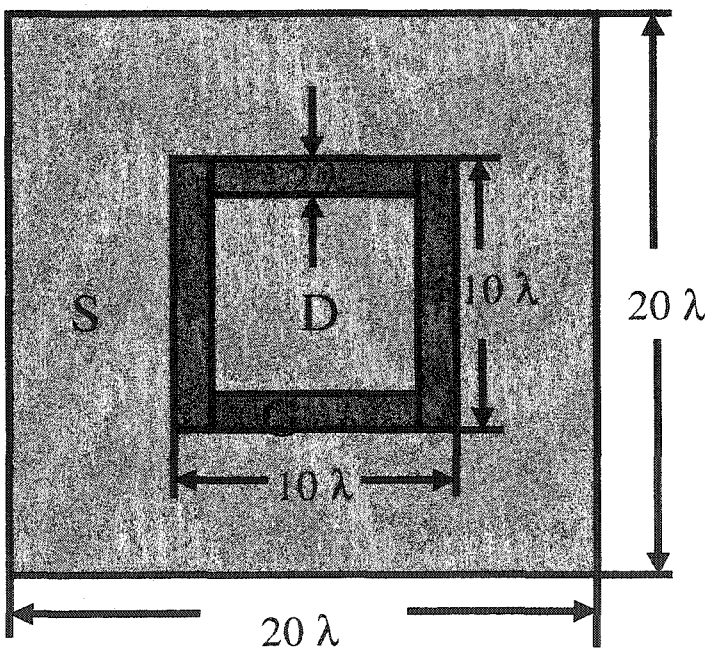


Figure 4.5: Concentric parallel cell layout

Table 4.1: The Influence of Different Layout

	Width of load transistor(μm)	VCO freq. convention layout(Hz)	VCO freq. Concentric layout
PMOS as active load	12.8	2.3G	2.8G
	19.2	2.7G	3.3G
	25.6	3G	3.7G
	32	3.2G	3.9G
	38.4	3.4G	4.1G

4.4.2 Method 2: Frequency enhancing with the NMOS load

In the conventional differential delay stage, NMOS transistors are used as the input drive transistors and PMOS transistors are used as the active loads. From the discussion in Section 4.3, we know that the VCO frequency increases with the transconductance per unit capacitance (gm/C) of the active load. Since the NMOS transistor has larger mobility than the PMOS transistor, the transconductance per unit capacitance of the NMOS transistors is larger than that of the PMOS transistors. So in order to further increase the VCO frequency, NMOS transistors are used as the active loads. Figure 4.6 is the schematic of the modified delay stage.

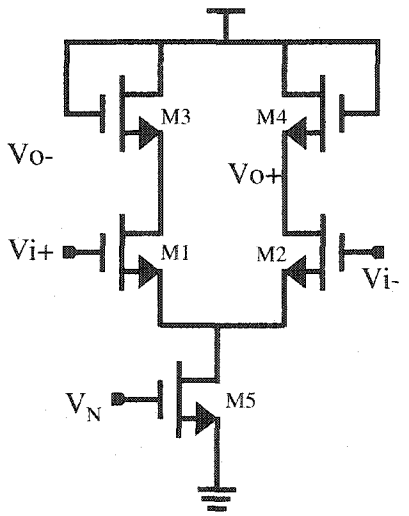


Figure 4.6: Delay cell using NMOS active load

Table 4.2 compares the VCO frequency at different active load for the conventional layout of Figure 4.4. In order to make a fair comparison, the size of the input transistor was fixed to $W_1=150\lambda$ and $L_1=2\lambda$.

From the simulation results, we can conclude that using NMOS transistor as the active load can increase the VCO frequency, provided that other conditions are kept the same as those when the PMOS transistor was used as the active load.

4.4.3 Method 3: Frequency enhancement combining method 1 & method 2

Table 4.3 shows the results by combining layout technique and load selection technique. From these results, a 4.8 GHz high operation frequency VCO is obtained using the HP 0.35μm CMOS process.

Table 4.2: The influence of the different load

active load size (W)	VCO freq. @ PMOS as active load	VCO freq. @ NMOS as active load
25λ	N/A	2.4GHz
50λ	2.45GHz	3.5GHz
75λ	2.75GHz	4.2GHz
100λ	3GHz	N/A

Table 4.3: The frequency enhancing using method 1 & method 2

Width of load transistor (μm)	VCO freq. with Concentric layout
6.4	3.3G
12.8	4.7G
15	4.8G

4.5 High Frequency VCO Design

A high frequency voltage control ring oscillator based upon NMOS loads with all transistors using concentric layout has been designed. Emphasis was placed on maximizing the speed of operation while still maintain quadrature outputs. The quadrature output criterion restricted the minimum value of n to 4. (With a complicated phase compensation circuit, two or three stages VCO with quadrature outputs also be reported recently [46][47].) The designed VCO is a 4-stages structure with $W_5=270\lambda$, $W_1=W_2=150\lambda$, $W_3=W_4=50\lambda$ and all $L= 2\lambda$. Simulation results based on 0.35μm CMOS process are shown in Figure 4.7. From these simulation results, it can be shown that the frequency can be as high as 4.85 GHz. If the quadrature output requirement was sacrificed, further enhancement of the oscillation frequency can be achieved by reducing the number of stages to 3 or, with appropriate modifications, to 2.

4.6 Conclusions

In this chapter, a high frequency ring VCO design has been presented. This design achieves frequency enhancement through minimization of diffusion parasitic capacitance with concentric layout and the transconductance density optimization. A 4-stage VCO designed in a 0.35μm CMOS process can operate in the frequency of 4.85 GHz.

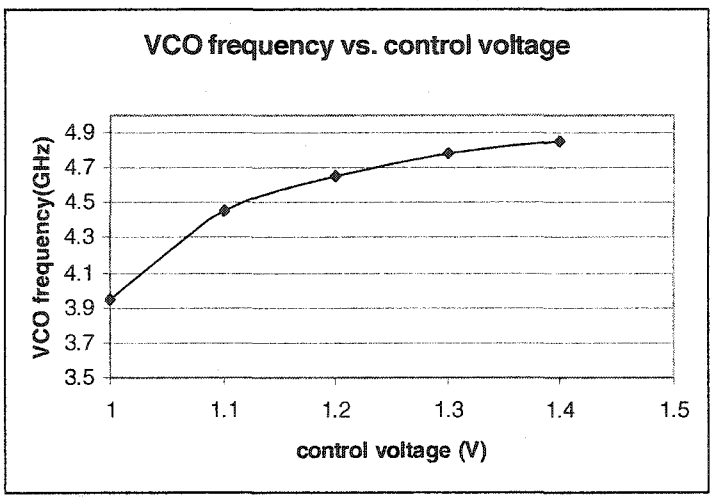


Figure 4.7: VCO frequency vs. control voltage

CHAPTER 5 HIGH FREQUENCY VCO-DERIVED FILTERS

5.1 Problem Definition and Motivation

In the past decades, integrated continuous-time filters have been successfully employed in a variety of applications ranging from low frequency to high frequency. In a wireless communication system, the operation frequency will be higher than 1 GHz. Attempts to reach higher operation frequencies have met with serious difficulties, related to the active-RC or g_m-c approaches.

It is well known that CMOS voltage controlled oscillators are capable of operating at very high frequencies. While reported continuous-time CMOS monolithic filters are invariably limited to operating frequency that are much lower than the reported oscillation frequencies of VCOs designed in the same process. By introducing additional loss in the delay stage of a VCO to move the poles into the left half-plane and appropriately introducing signal inputs into the resultant structure, monolithic filters that have operation frequencies comparable to the oscillation frequency of the VCO can be derived.

5.2 Literature Review

Integrated analog filters can be classified into two categories: continuous-time filters and discrete-time filters. Continuous-time filters are capable of operating at higher frequency than the discrete-time filters but this often cost linearity and noise performance. However, there are many applications in the areas of direct signal processing in which the distortion and noise performance requirements are relaxed [48]. A good example of an appropriate application of continuous-time filters in direct signal processing is the read channel of disk drives [49][50]. Other applications for direct signal processing include wireless communication systems [51], and loop filters for phase-locked loops [52]. The operation frequency of the continuous-time filters in these applications varies from a few hertz (for loop filters) to hundreds of Megahertz (for disk drive read channels), and even to a few Gegahertz (in wireless applications). The dynamic range of these filters varies from 40 to 70dB.

In the continuous-time filter domain, g_m-C filters offer a speed advantage over active R-C and MOSFET-C filters. The basic building block of g_m-C filter is an integrator involving a transconductor and a capacitor or a bank of capacitors. The frequency of g_m-C filter is proportional to the unit-gain frequency of the integrator, which is much higher than the bandwidth of OP AMP used in the active R-C or MOSFET R-C filters.

For filters with frequency higher than 1 GHz, L-C filters are usually employed [53]-[55]. L-C filters often need external inductors. Recently, the technique of fully integrated spiral inductor on chip substrate makes the monolithic L-C filter possible. But due to the parasitic effects, only low-quality inductors can be achieved. On the other hand, the inductors on chip occupy a substantially larger area, and this decreases the yield and also increases the fabrication cost. An alternative way to make an inductor is using the bonding wire. This technique increases the quality factor of the LC tank, but it is not accepted in the industry due to the lack of yield repeatability.

Reported continuous-time CMOS monolithic filters are invariably limited to operation frequency that are much lower than the reported oscillation frequencies of VCOs designed in the same process. In high frequency voltage ring oscillators, operation frequency is proportional to g_m/c, where g_m is the transconductance of driving transistor, and c is the output node parasitic capacitance in the delay stage. Comparing to g_m-C filter, the parasitic capacitance in the delay stage of the VCO is much less than the load capacitance in the integrator of the filter. So VCO has the potential to operate faster than the g_m-c filter.

5.3 VCO-Derived Filter Design

A ring voltage controlled oscillator is generally realized by cascading an odd number of open-loop inverting amplifiers (often termed "delay stages" when used in VCOs) in a feedback loop or a "ring". An even number of delay stages can also be used provided that an odd number of amplifiers in the ring are noninverting. The amplifiers have signal propagation delay approximately half of the period of the oscillation frequency. These delay stages are often simply integrators which invariably have some loss either introduced intentionally or attributable to the non-zero output conductance of the MOS transistors. In some VCO's, feedback or control mechanisms are used to control this loss which affects both

the waveshape and frequency of the VCO output signal. The small-signal pole locations of the VCO are dependent on the amount of loss in the delay stages with a requirement that at least one complex-conjugate pole-pair be in the right half-plane to sustain oscillation of the VCO. If too much loss is added in the delay stages, oscillation will cease and the VCO will behave as a filter if signal inputs are added appropriately.

In the filter terminology, the delay stages are generally termed lossy integrators. In this chapter, we will use the word "integrator" and "lossy intergrator" in both VCO and filter cases. The lossy integrators generally have dominantly a first-order small signal transfer function with the transfer function given by

$$\frac{V_o}{V_i} = \frac{I_o}{s+p} \tag{5.1}$$

Where I_o is the unity-gain frequency, and pole p is the loss term.

It can be shown that an n-stage VCO constructed with identical lossy integrators has poles on a circular constellation located at

$$s = (-1)^{1/n} I_0 - p \tag{5.2}$$

The location of the pole constellation of the system can be controlled by modifying the amount of integrator loss. Increasing the loss pushes the pole constellation leftward in the s-plane while reducing the loss will move the constellation rightward. Thus by appropriately controlling the loss, the poles can be placed in the LHP ensuring a stable system. Figure 5.1 illustrates a 3-stage VCO's pole constellation with and without additional loss.

Based on this concept, a VCO-derived low-pass filter can be designed by moving the pole constellation by the proper amount to the left and adding an external input to one of the lossy integrators. Figure 5.2 shows the block diagram of the 3-stage VCO-derived low-pass filter. Where V_P and V_N are the control voltages, V_{i+}, V_{i-} are the inputs and V_{o+}, V_{o-} are the outputs.

The transfer function of this low pass filter is

$$\frac{X_o}{X_i} = -\frac{I_0^3}{(s+p)^3 + I_0^3} \tag{5.3}$$

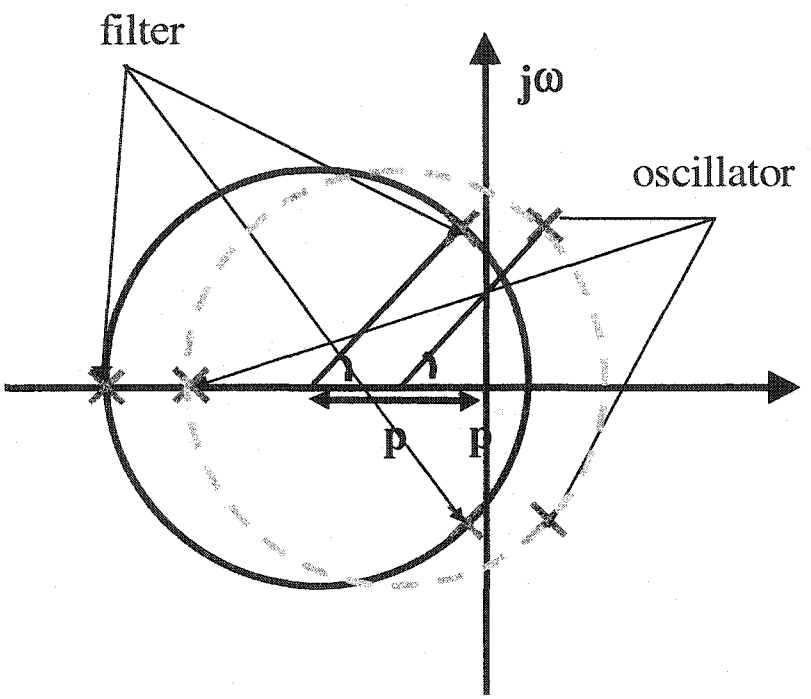


Figure 5.1: The poles location of the 3-stage oscillator (without additional loss) and filter (with additional loss)

This can be expressed as

$$\frac{X_o}{X_i} = -\frac{I_0^3}{\left(s^2 + \frac{\omega_0}{Q}s + \omega_0^2\right)(s + p_3)} \tag{5.4}$$

For high Q poles, the transfer function can be approximated by the second-order function

$$\frac{X_o}{X_i} \cong -\frac{I_0^2}{\left(s^2 + \frac{\omega_0}{Q}s + \omega_0^2\right)} \tag{5.5}$$

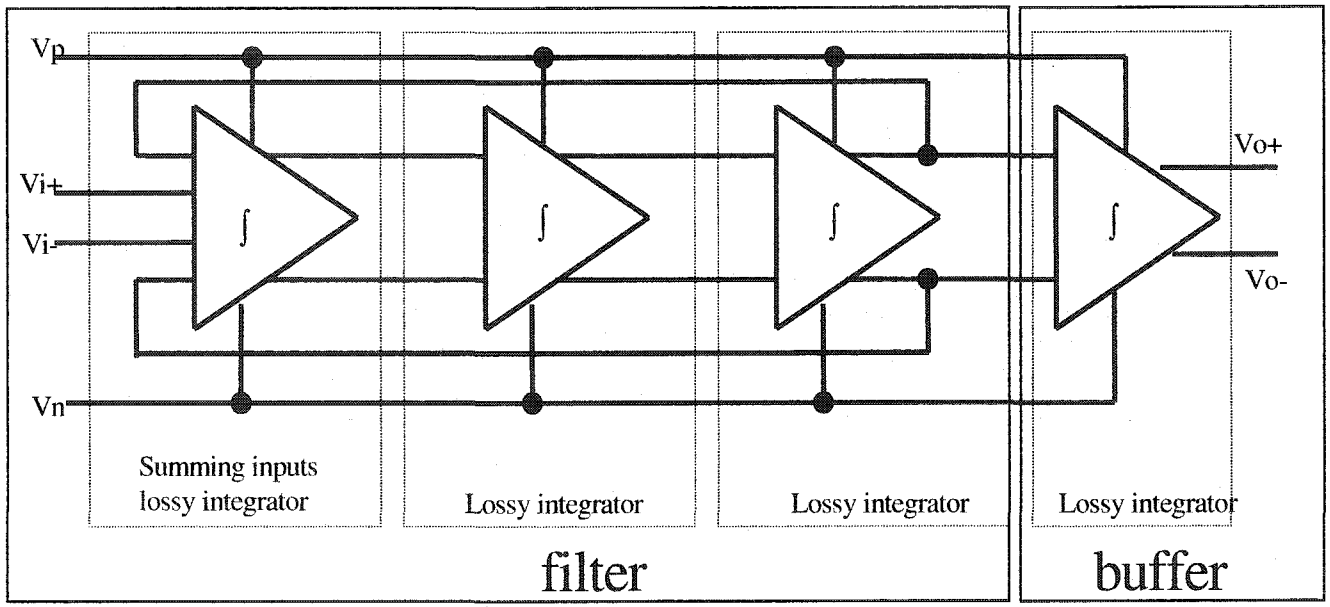


Figure 5.2: The diagram of the 3-stage VCO-derived low-pass filter

A band-pass filter can be created by adding a zero near the origin. One way to achieve this is by making the last integrator stage lossless and obtaining the filter's output from the second last stage. The block diagram of a 3-stage band-pass filter is shown in Figure 5.3.

The band-pass filter transfer function can be approximated by a second-order function

$$\frac{X_o}{X_i} \cong -\frac{I_0^2 s}{\left(s^2 + \frac{\omega_0}{Q} s + \omega_0^2\right)} \tag{5.6}$$

5.4 Components Design

To implement a low-pass VCO-derived filter, a lossy integrator with summing inputs and a lossy integrator without summing inputs are required. The band-pass filter implementation requires a lossless integrator in addition to the two integrators required in low-pass filters. To achieve low noise and distortion, the fully differential structures are used. These integrators will be discussed next.

5.4.1 Lossless integrator

A lossless or low lossy integrator is required to implement the band-pass filter in order to provide a zero at the origin. A widely usage VCO delay stage that is actually a low loss integrator is shown in Figure 5.4. M1-M5 form the core of a lossless integrator and M6-M13 form the common mode feedback circuit. Due to the non-infinity impedance of the current source formed by M3 and M4, the zero of the band-pass filter will not exactly on the origin. Table 5.1 shows the transistors sizes of the lossless integrator in the band-pass filters.

5.4.2 Lossy integrator

The widely used VCO delay stage that behaves as a lossy integrator is shown in Figure 5.5 Compared to the low-loss integrator, the lossy integrator has a pair of diode connected active loads paralleled with the PMOS adjustable current source. The controlled voltages, which are used in a VCO to control the frequency of oscillation, V_n and V_P control the unity-gain frequency and the loss of the integrator. In low-pass filter, in order to increase

the cutoff frequency of the filter, M3 and M4 are removed to decrease the output node capacitance. Table 5.2 and Table 5.3 show the transistors sizes of the lossy integrator in the low-pass filter and band-pass filter, respectively.

5.4.3 Lossy integrator with summing inputs

A lossy integrator with summing inputs was constructed by adding an additional input pair to the lossy integrator shown in Figure 5.5. The resultant schematic is shown in Figure 5.6. Again, M3 and M4 in the low-pass filter are removed to increase the cutoff frequency. Table 5.4 and Table 5.5 show the transistors sizes of the lossy integrator with summing inputs in low-pass and band-pass filter, respectively.

Table 5.1: The transistors sizes of the lossless integrator in the band-pass filter

W1/L1	W2/L2	W3/L3	W4/L4
14u/250n	14u/250n	18u/250n	18u/250n
W5/L5	W6/L6	W7/L7	W8/L8
40u/250n	40u/250n	40u/250n	1u/250n
W9/L9	W10/L10	W11/L11	W12/L12
1u/250n	4u/250n	4u/250n	28u/250n
W13/L13	W14/L14	W15/L15	W16/L16
28u/250n	10u/250n	40u/250n	1u/250n

Table 5.2: The transistors sizes of the lossy integrator in low-pass filter

W1/L1	W2/L2	W5/L5	W6/L6	W7/L7
18u/250n	18u/250n	35u/250n	35u/250n	60u/250n

Table 5.3: The transistors sizes of the lossy integrator in band-pass filter

W1/L1	W2/L2	W3/L3	W4/L4
14u/250n	14u/250n	30/250n	30u/250n
W5/L5	W6/L6	W7/L7	
6u/250n	6u/250n	40u/250n	

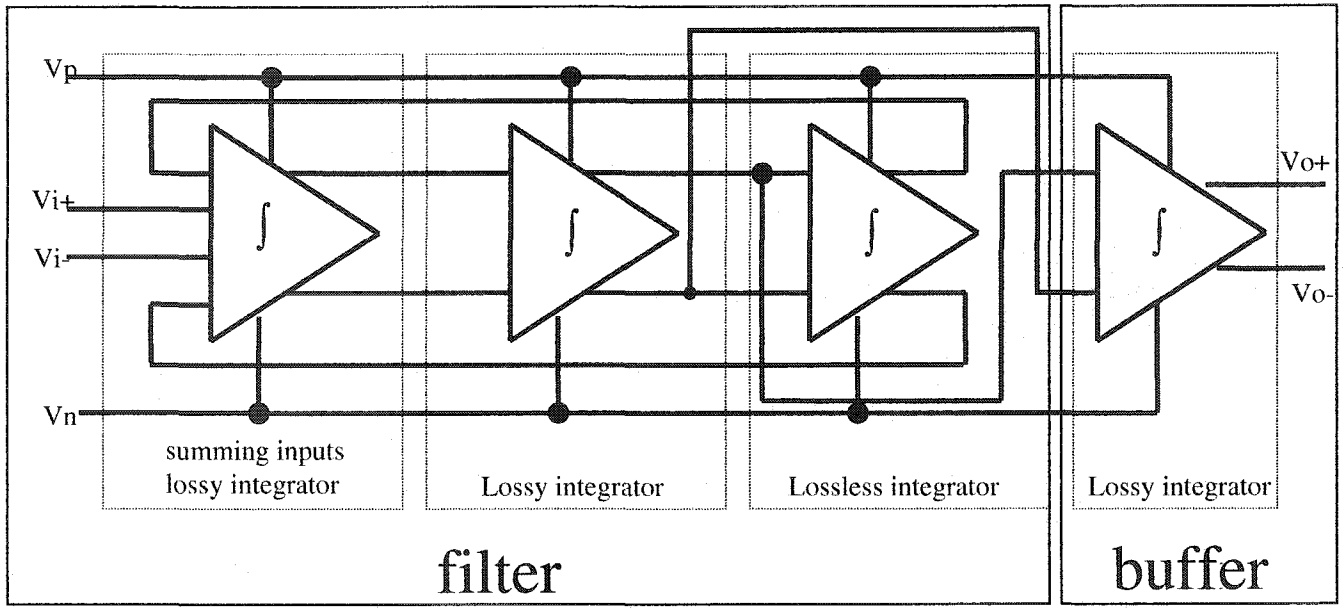


Figure 5.3: The diagram of a 3-stage VCO-derived band-pass filter

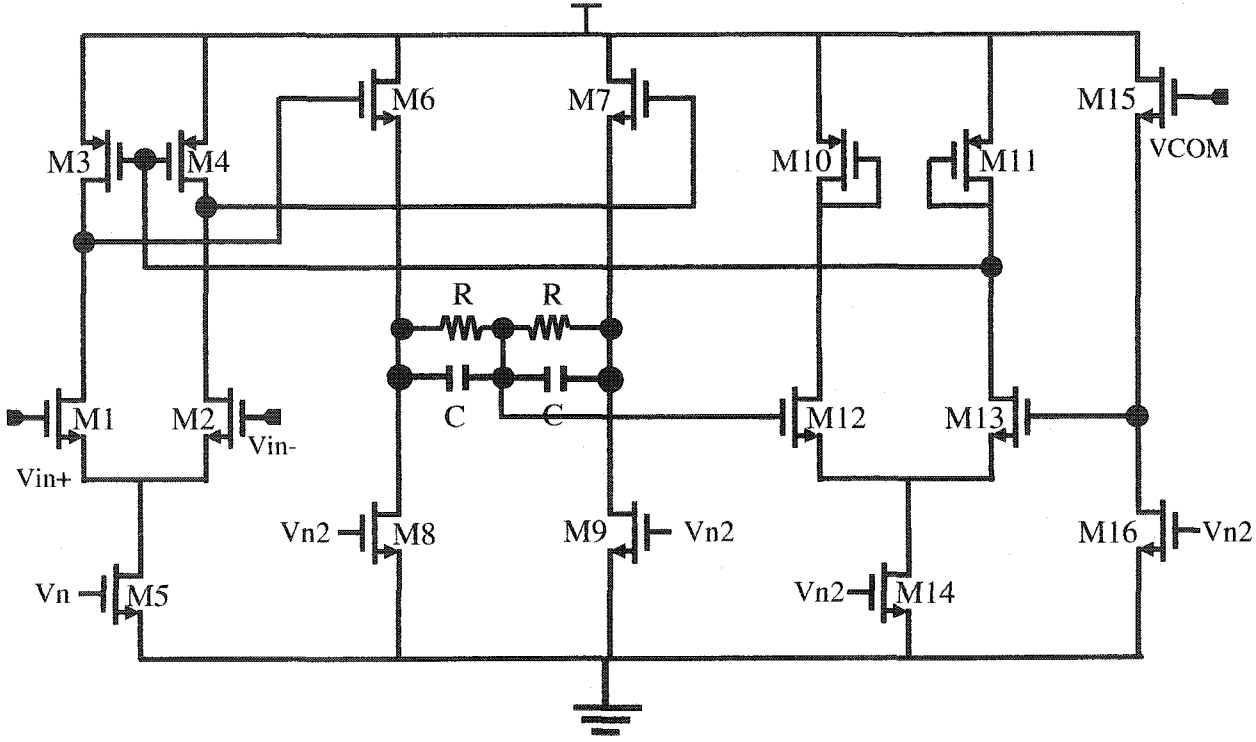


Figure 5.4: The schematic of low loss integrator for band-pass filter

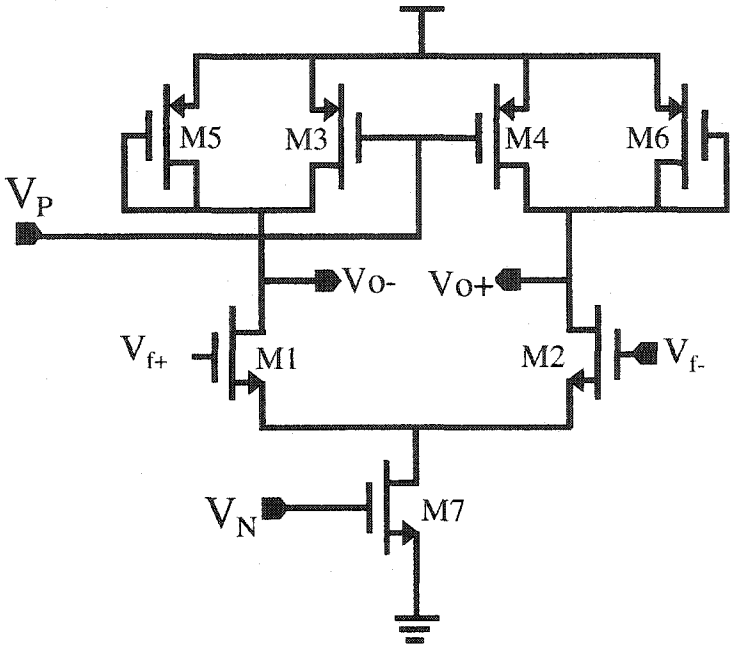


Figure 5.5: The schematic of the lossy integrator

Using the integrators shown in this section, it can be shown with a tedious derivation that the Q and ω_o of a low-pass or band-pass filter can be expressed as

$$Q = \frac{\sqrt{1 - 2\cos\theta \cdot \frac{g_{m5}}{g_{m1}} + \left(\frac{g_{m5}}{g_{m1}}\right)^2}}{2\left(\cos\theta - \frac{g_{m5}}{g_{m1}}\right)} \tag{5.7}$$

$$\omega_o = \frac{g_{m1}}{C_L}\sqrt{1 - 2\cos\theta \cdot \frac{g_{m5}}{g_{m1}} + \left(\frac{g_{m5}}{g_{m1}}\right)^2} \tag{5.8}$$

Where g_{m1} and g_{m5} are the transconductances of M1 and M5 in Figure 5.6: The schematic of the lossy integrator with summing inputs., respectively, C_L is the total capacitance on the output node of the integrator and where θ is a constant depending on the number of delay stages in the parent VCO which in this example is assumed to be three. For the three-stage oscillator, $\theta=60°$.

Table 5.4: The transistors sizes of the lossy integrator with summing inputs in low-pass filter

W1/L1	W2/L2	W5/L5	W6/L6
18u/250n	18u/250n	35u/250n	35u/250n
W9/L9	W10/L10	W7/L7	
36u/250n	36u/250n	60u/250n	

Table 5.5: The transistors sizes of the lossy integrator with summing inputs in band-pass filter

W1/L1	W2/L2	W3/L3	W4/L4
14u/250n	14u/250n	30u/250n	30u/250n
W5/L5	W6/L6	W7/L7	W9/L9
6u/250n	6u/250n	40u/250n	14u/250n
W10/L10			
14u/250n			

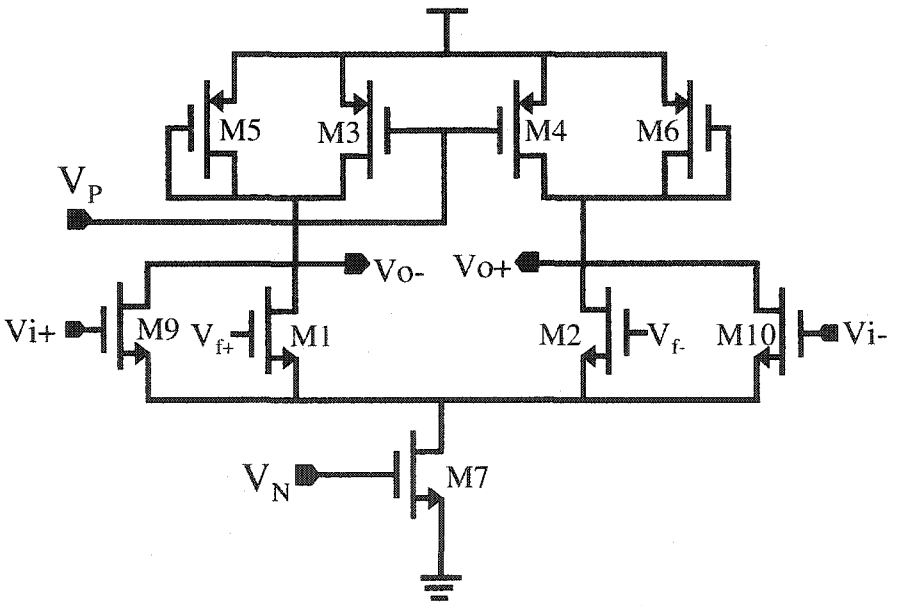


Figure 5.6: The schematic of the lossy integrator with summing inputs.

5.5 Simulation Results

The circuit was designed for the TSMC 0.25μm process and was simulated using the Hspice simulator.

5.5.1 Low-pass filter

A low-pass filter with a -3 dB bandwidth of 4.3 GHz at normal process corner and normal temperature was designed. The AC and transient response are shown in Figure 5.7 and Figure 5.8 respectively. Figure 5.9 shows the frequency spectrum of the output signal with a single-end output swing of 200 mV and a frequency of 3 GHz. The THD is around –40dB.

5.5.2 Band-pass filter

A band-pass filter with a center frequency that is tunable from 2.28 GHz to 3.11 GHz and a Q factor that is adjustable from 3 to 85 was also designed. The performance of the designed band-pass filter is summarized in Table 5.6. The AC responses of a sample band-pass filter with a Q of 5 and a center frequency of 2.3 GHz is shown in Figure 5.10. Figure 5.11 shows the transient response of above band-pass filter excited by a sinusoid signal with a frequency of 2.3 Ghz and a single-end output swing around 80mV. Figure 5.12 shows the frequency spectrum of the output signal with the single-end output swing of 80 mV. It exhibits a THD of –40dB.

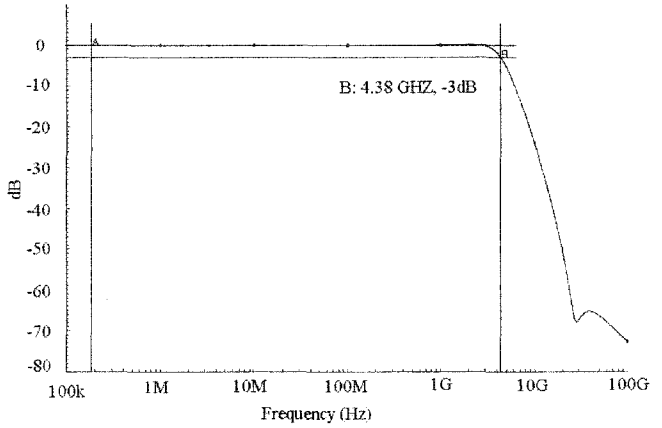


Figure 5.7: The AC response of a sample low-pass filter

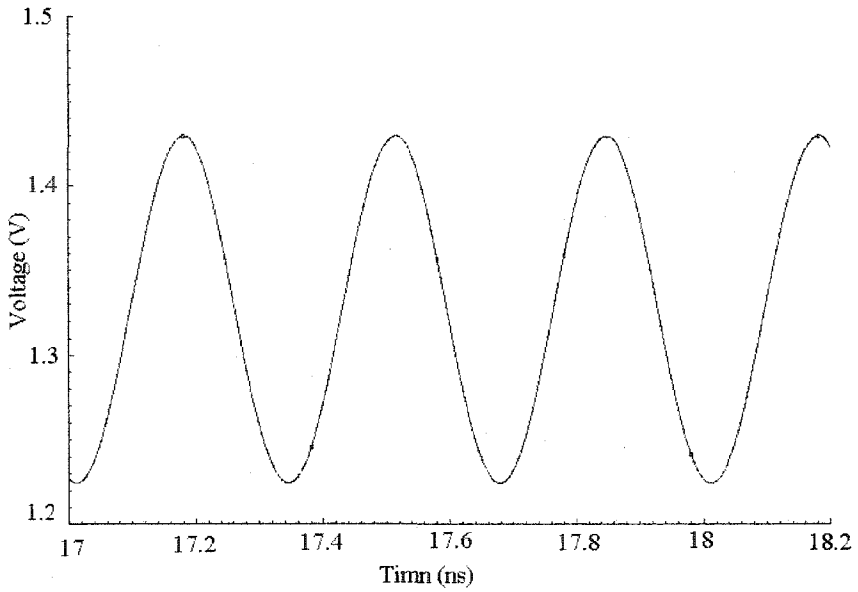


Figure 5.8: The transient response of the low-pass filter in Figure 5.7

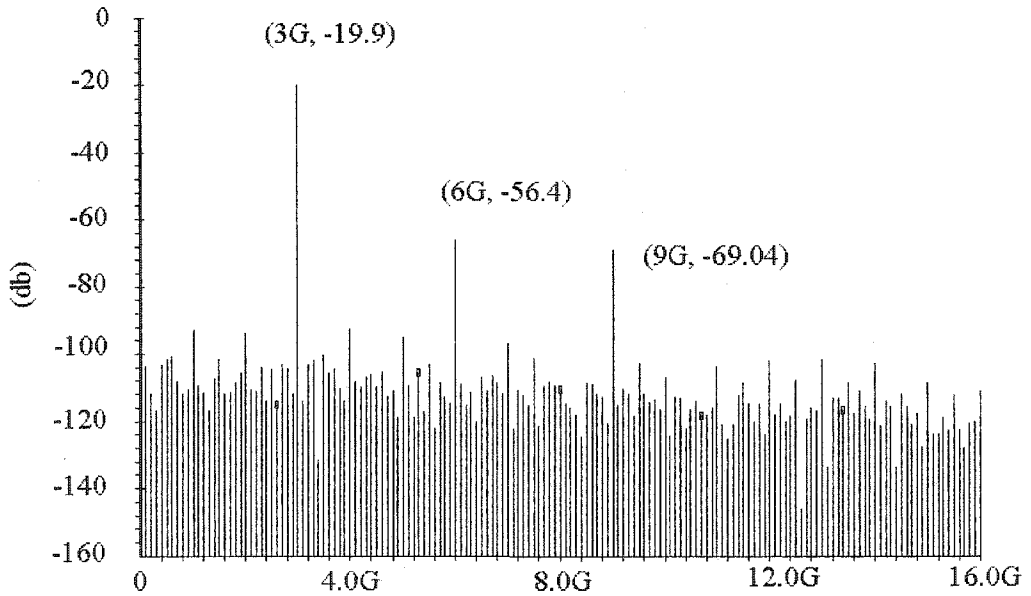


Figure 5.9: The frequency spectrum of the low -pass filter, single-end output swing is 200 mV.

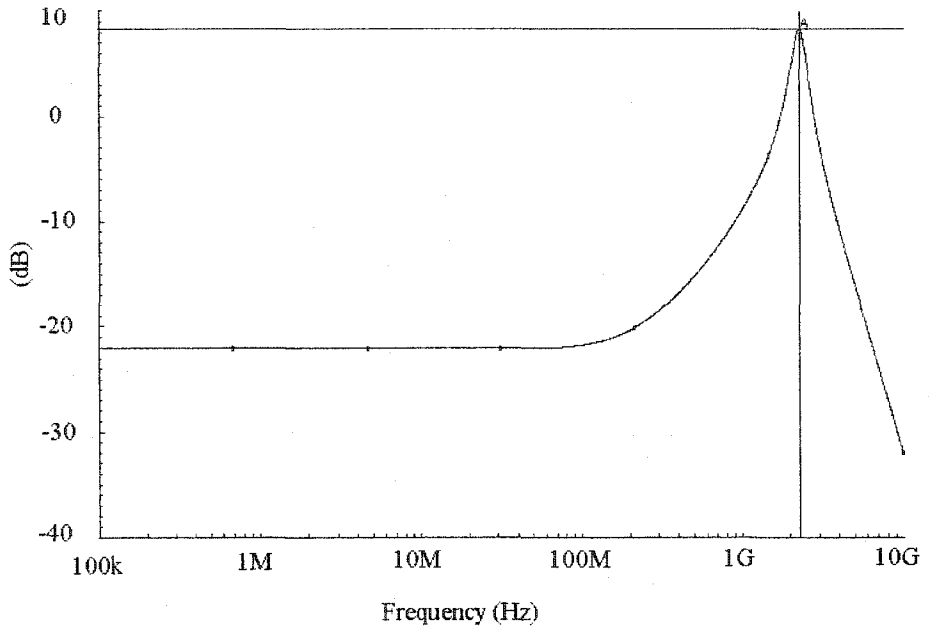


Figure 5.10: The AC response of a sample band-pass filter.

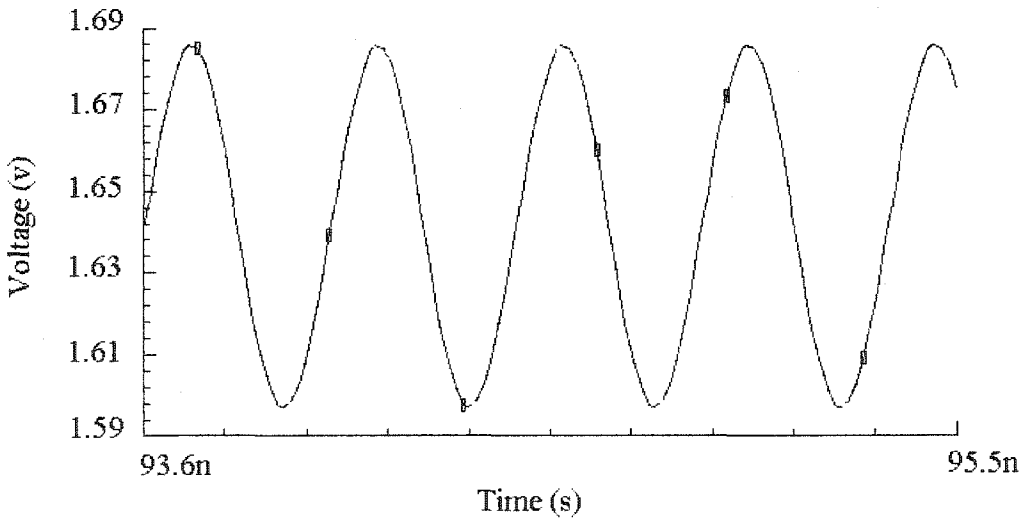


Figure 5.11: The transient response of the band-pass filter with a 80mV single-end output swing.

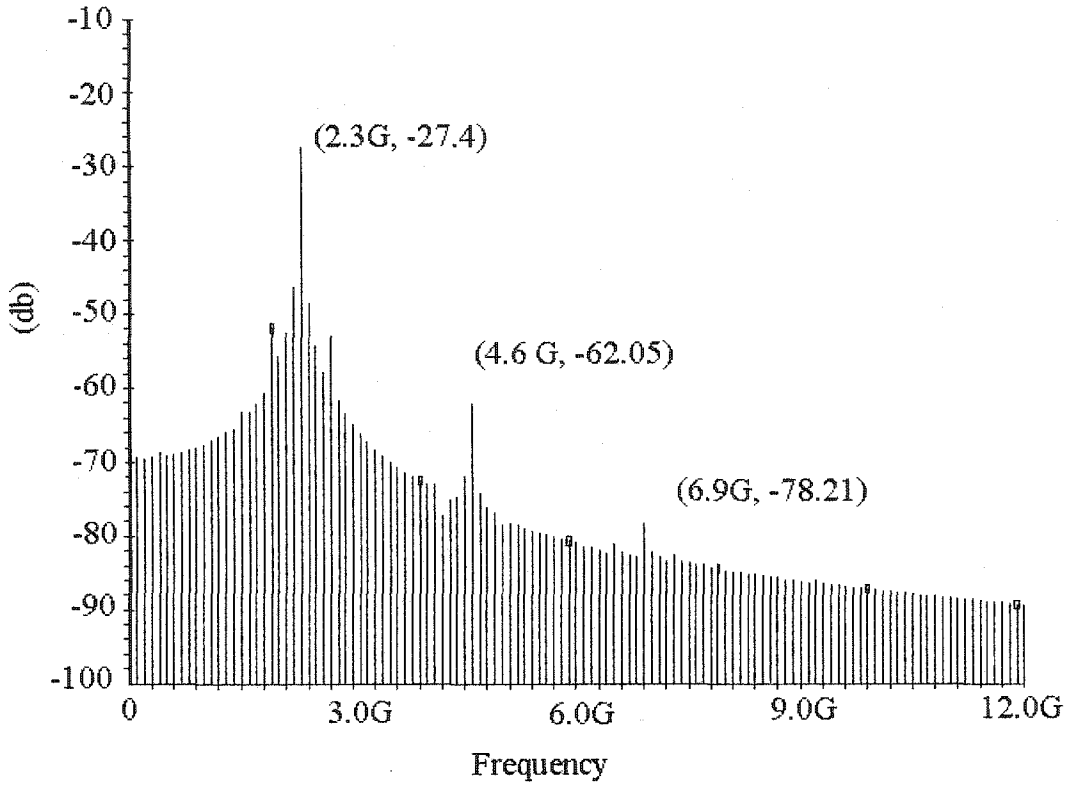


Figure 5.12: The frequency spectrum of one band-pass filter

5.6 Conclusions

A method of designing monolithic filters derived from CMOS VCOs was introduced. A sample of the VCO-derived low-pass filters and a sample of the band-pass filters were presented. A low-pass filter with a cut-off frequency of 4.3 GHz was designed in the TSMC CMOS 0.25 μm process. It exhibits a THD of – 40dB with a 200mV single-end output swing. A band-pass filter with a center frequency tunable from 2.28 GHz to 3.11 GHz and a Q adjustable from 3 to 85 was also designed. It exhibits a THD of –40dB with an 80mV single-end output swing. The VCO-derived filters offer two main advantages over other types of integrated CMOS filters: higher operation frequency, and a higher and easily adjustable Q. VCO-derived filters offer potential for use in modern communication circuits that require modest distortion performance.

Table 5.6: Simulated performance of the designed band-pass filter

V_n (V)	V_p (V)	ω_0(GHz)	Q
0.7	2	2.28	5.0
	1.8	2.29	6.1
	1.6	2.33	14.3
	1.525	2.34	27.0
	0	2.34	52.0
0.8	2	2.74	3.1
	1.8	2.75	3.4
	1.6	2.81	4.0
	1.4	2.81	5.7
	1.2	2.85	11.9
	1.05	1.88	84.6
0.9	2	2.99	2.4
	1.6	3.03	2.6
	1.4	3.05	2.9
	1.0	3.10	4.3
	0.6	3.11	7.2
	0.2	3.11	8.6
	0	3.11	9.2

CHAPTER 6 CURRENT MIRROR CIRCUIT WITH ACCURATE MIRROR GAIN FOR LOW β TRANSISTORS

6.1 Problem Definition and Motivation

The current mirror is one of the most basic building blocks used in linear IC design. Although CMOS process have become dominant in applications requiring a large amount of digital circuitry on a chip, BJT circuits in either Bi-CMOS or bipolar processes remain popular for high-speed applications due to the very high unity-gain frequencies attainable with modern bipolar transistors. Unfortunately, in bipolar transistors, the base control terminal draws a nonzero input current. Specially, for lateral transistor, the base current in some processes may be as large as 20% (for $\beta = 5$) of the collector current. In a simple bipolar current mirror with $\beta = 5$, the base current will cause a 30% error in current mirror gain. There are several known approaches for minimizing the base current effects. Most are suitable for high β transistors where the detrimental effects of base current loss on mirror gain are already modest. For low β transistors, most existing methods show either poor accuracy or poor frequency response.

In this chapter, a new approach for designing bipolar current mirrors is presented. The new current mirror has smaller gain errors due to base current loss than previously reported structures and is most beneficial when an accurate mirror gain is required from low β transistors. The new current mirrors can be implemented in bipolar or Bi-CMOS processes or in CMOS process with the parasitic bipolar transistors.

6.2 Literature Review

A simple bipolar current mirror structure is shown in Figure 6.1 [56]. In this structure, a constant current source I_{in} is fed into the collector of the diode-connected transistor Q1 establishing a voltage across the base-emitter junction of Q1. This voltage is applied across the base-emitter terminals of Q2. If Q1 and Q2 are matched, the emitter currents of Q1 and Q2 will be the same. If the base currents of Q1 and Q2 are negligibly small, it follows that

the output current I_{out} will be the same as the input current. If the base currents are not negligibly small, this current mirror has an output current I_{out} that is smaller than the input current because a current whose value is equal to the sum of base currents of Q1 and Q2 is subtracted from the input current before it reaches the collector of Q1. Taking these two base currents into account and assuming Q1 and Q2 are perfectly matched, the current mirror gain is given by

$$A = \frac{I_{out}}{I_{in}} = \frac{1}{1+\frac{2}{\beta}} \tag{6.1}$$

where β is the transistor current gain of Q1 and Q2.

The current mirror gain error is defined by the expression

$$GainError = \left| \frac{A - A_{nom}}{A_{nom}} \right| \times 100(\%) \tag{6.2}$$

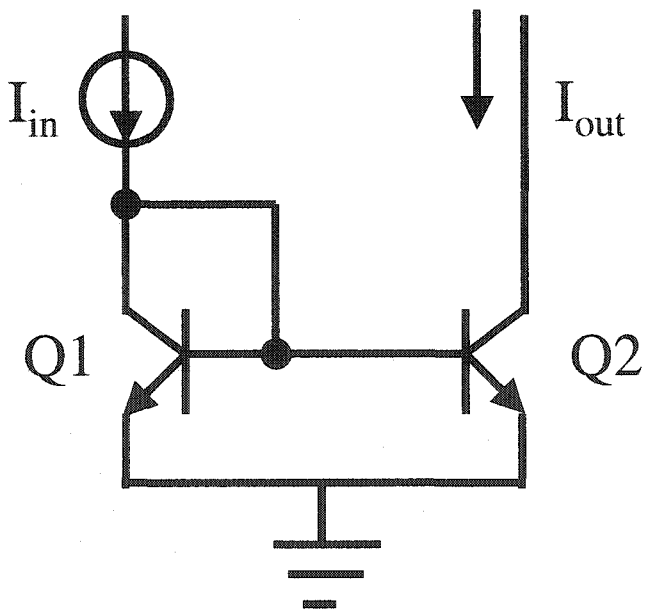


Figure 6.1: The simply bipolar current mirror

For lateral transistors, β is often in the range of only 4 to 20. For such transistors, the current mirror gain error is too large for most applications. For example, the current mirror gain error from Equation (6.2) will be 30% if $\beta = 5$.

A well-known modification of the simple current mirror that partially compensates for base current loss is shown in Figure 6.2. An emitter-follower buffer, Q3, is included between emitter and base of Q1. The sum of the base currents of Q1 and Q2 is divided by (β+1) of Q3 resulting in a smaller current that has to be subtracted from the input current I_{in}. Assuming $\beta_1=\beta_2=\beta_3=\beta$, then the current mirror gain of the circuit in Figure 6.2 is given by

$$A = \frac{I_{out}}{I_{in}} = \frac{1}{1+\frac{2}{\beta^2+\beta}} \cong \frac{1}{1+\frac{2}{\beta^2}} \tag{6.3}$$

For $\beta=5$, the current mirror gain error will be around 7%.

To further minimize the base current effect, the Darlington configuration can be used to achieve a larger current gain in the feedback amplifier. The current mirror structure based upon the Darlington compensation is shown in Figure 6.3. For this structure, the sum of the base currents of Q1 and Q2 is divided by $(\beta+1)^2$ resulting in a much smaller current that has to be subtracted from the input current I_{in}. Again assuming all the transistors are matched, the current mirror gain is given by

$$A = \frac{I_{out}}{I_{in}} = \frac{1}{1+\frac{2}{\beta^3+2\beta^2+\beta}} \cong \frac{1}{1+\frac{2}{\beta^3}} \tag{6.4}$$

For $\beta=5$, the current mirror gain error will be about 1.6%.

Although this structure does offer improvements in mirror gain accuracy, this current mirror has a poor high frequency response due to the fact that base current of Q3 is small and it takes long time to charge the parasitic capacitances at the base of Q3.

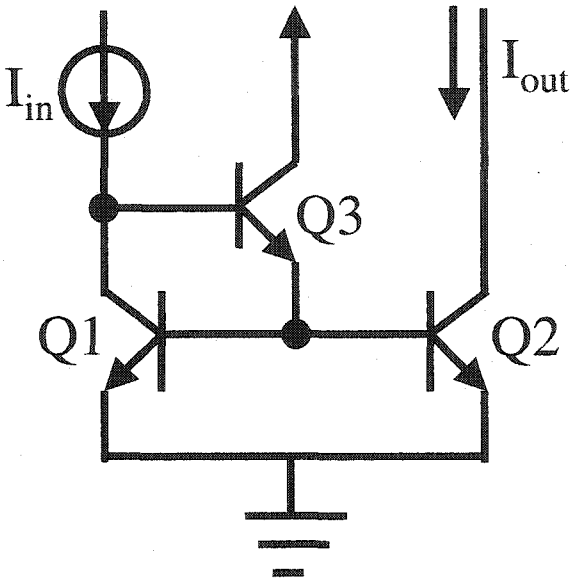


Figure 6.2: A current mirror with an emitter-follower buffer to provide base current compensation.

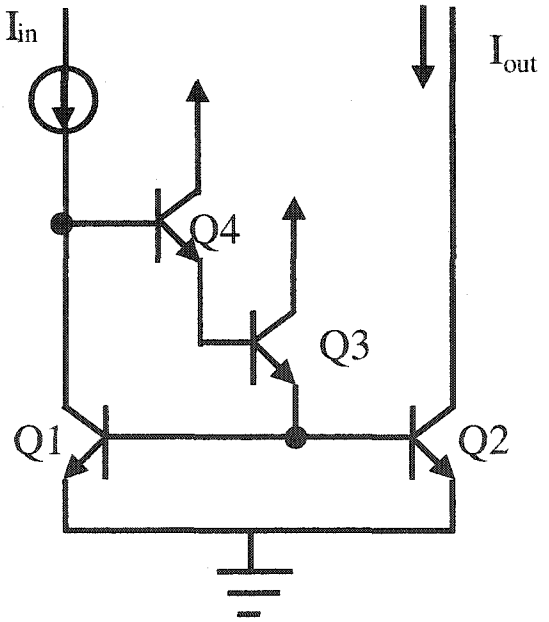


Figure 6.3: A current mirror with Darlington configuration to compensate for the base currents

In the BiCMOS processes, an NMOS transistor can be added to compensate for the base currents [10]. The simple structure is shown in Figure 6.4. If Q1 and Q2 are perfectly matched, this current mirror has an output current I_{out} exactly equal to the input current I_{in} due to the fact that no base current is subtracted from the input current. Unfortunately, the MOS transistor is not available in standard bipolar processes.

A bipolar transistor with a split-collector can be used to improve the current match between the input and output of the current mirror [11]. The split-collector current mirror structure is shown in Figure 6.5. A single split-collector transistor Q4 is used in this structure. The emitter of Q4 is connected to the common base of the transistors Q1 and Q2, the base terminal of Q4 is connected to collector of Q2, and one part of the split collector of Q4 is also connected to the collector of Q2. The other part of the split collector is directly connected to output. The cascoding transistor Q3 provides a high impedance at the output node and also provides a compensation current to I_{in}. A routine analysis shows that the current mirror gain is given by the expression (6.5)

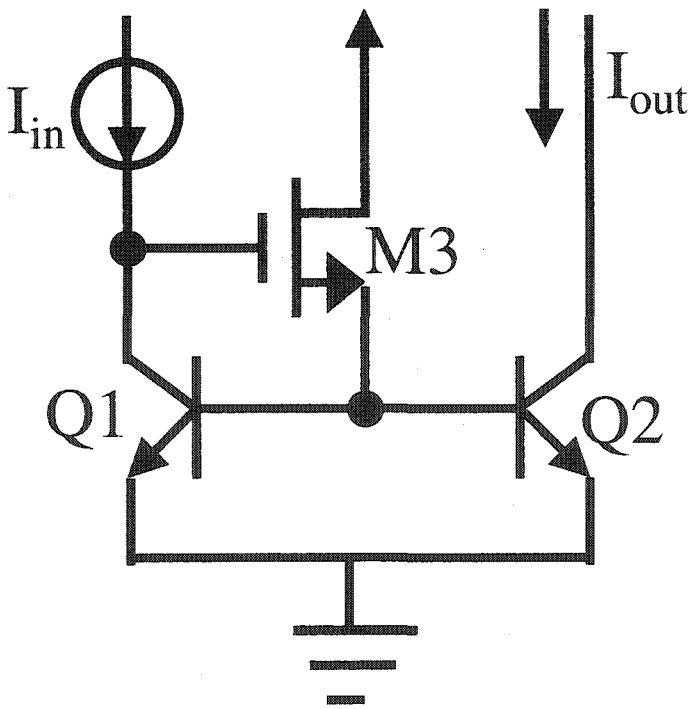


Figure 6.4: A current mirror with a MOS transistor to compensate for the base current

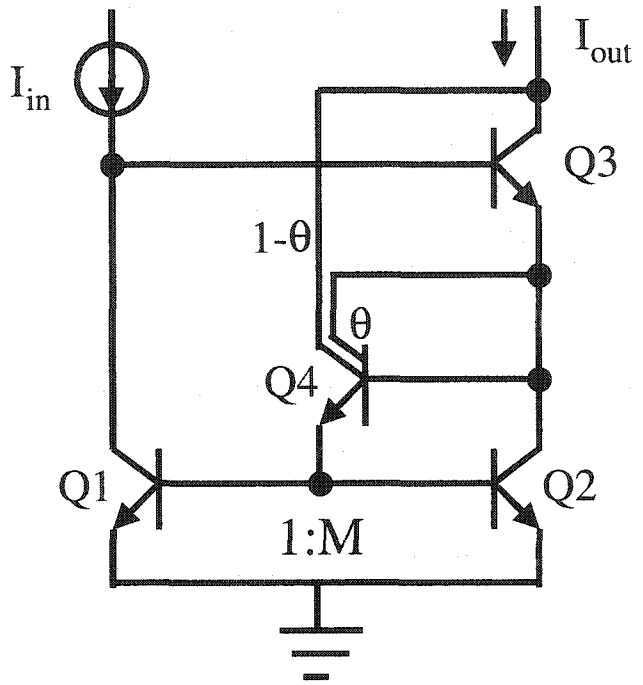


Figure 6.5: A current mirror with a split-collector BJT to compensate for the base currents

$$A=\frac{I_{out}}{I_{in}}=\frac{M-(M-1)*\frac{1}{1+\beta}+[(1-\theta)M-\theta]*\frac{1}{(1+\beta)^2}-(1+M)(1-\theta)*\frac{1}{(1+\beta)^3}}{1+(M-1)*\frac{1}{1+\beta}-[(1-\theta)M-\theta]*\frac{1}{(1+\beta)^2}+(1+M)(1-\theta)*\frac{1}{(1+\beta)^3}} \quad (6.5)$$

where M is the ratio of the emitter areas of Q2 to Q1 and θ is the collector current split factor. For M=1 and θ=1/2, the mirror gain expression of (6.5) reduces to

$$A=\frac{I_{out}}{I_{in}}=\frac{1-\frac{1}{(1+\beta)^3}}{1+\frac{1}{(1+\beta)^3}} \quad (6.6)$$

For β= 5, then the mirror gain error is about 0.92%.

Although the split-collector mirror gain is much more accurate than what is achievable with either the basic mirror or the base current compensated structure from Figure 6.2-6.4, this mirror can get good current matching only when M is 1. For mirror gains larger than 1, the first-order $(1+\beta)$ terms of the numerator and denominator in Equation (6.5) no longer disappear and become dominant resulting in a large error in the mirror gain. For example, when M=2, the mirror gain error is around 30% for $\beta = 5$.

6.3 Proposed Current Mirror

A new current mirror structure is shown in Figure 6.6. In this structure, the base current loss is compensated by ideally subtracting a corresponding current from the output current. To achieve this, one split collector of Q3 is directly connected to the output and the other split collector is connected to the emitter of Q4. Part of the collector current is divided by $(\beta+1)$ of Q4 and then subtracted from I_{out}. Assuming that all transistors have the same β, the current mirror gain is given by

$$A = \frac{I_o}{I_{in}} = M \cdot \frac{1 + \frac{(1+M)}{(1+\beta)} \cdot \frac{1}{M} \cdot \left[(1-\theta) + \frac{\theta}{(1+\beta)} \right]}{1 + \frac{(1+M)}{\beta \cdot (1+\beta)}} \qquad (6.7)$$

where M is the ratio of the emitter areas of Q2 to Q1. It follows from (6.7) that the current mirror gain is exactly equal to M when $\theta = \frac{(1+\beta)(\beta - M)}{\beta^2}$. M has to be smaller than β to satisfy the condition of $0<\theta<1$.

Due to process variations, the value of β may be different from its nominal value. Table 6.1 shows the current mirror gain error for the new circuit due to process variations of ± 20% and ± 30% for several different mirror gains and several different nominal β.

From Table 6.1, it is apparent that the mirror gain error is higher for lower β and higher M. For $M=1$ and $\beta=5$, the gain error is 1.28%, which is comparable to Mesa's work [11]. For mirror gains greater than 1, the proposed current mirror gives much smaller mirror gain errors than the circuit shown in Figure 6.5.

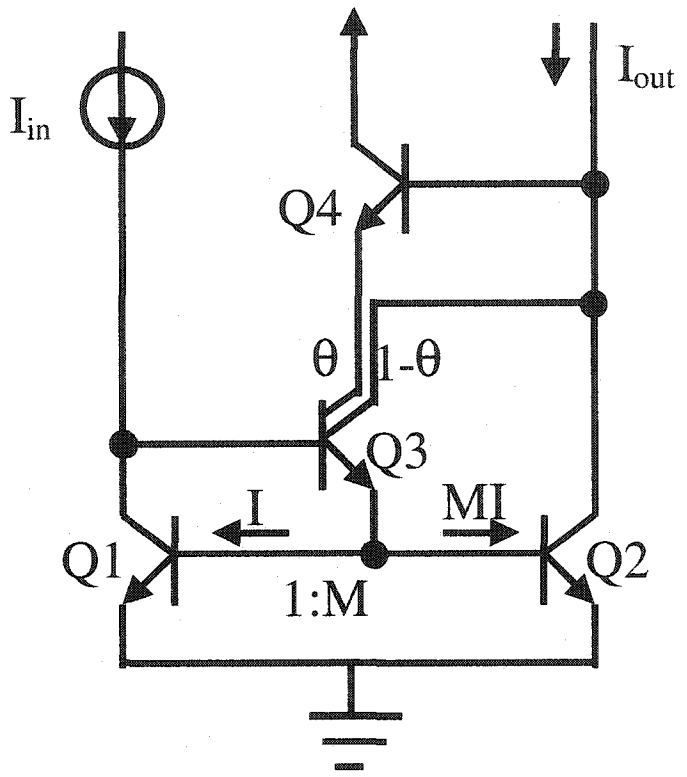


Figure 6.6: A current mirror with a split-collector transistor to compensate for the base currents

Two issues of concern when designing any current mirror are the mirror gain accuracy and the output impedance of the current mirror. Multiple output current mirrors are also required in some applications. Two modifications of the basic circuit shown in Figure 6.6 will be discussed. One version has a high impedance output and another has the multiple outputs. Both have good current mirror gain accuracy even with the low values of β.

6.4 Proposed Current Mirror with High Output Impedance

To increase the output impedance, a cascode version of above design is introduced. This current mirror has higher output impedance and better current matching. Figure 6.7 shows the modified current mirror structure. Various known methods can be used to generate the bias voltage, $V_{bias.}$ which is used to bias the cascode transistors.

$$\frac{I_o}{I_{in}} = M \cdot \frac{1+\frac{(1+M)}{\beta^2}\cdot\frac{\beta}{M}\cdot\left[\theta+\frac{1-\theta}{(1+\beta)}\right]}{1+\frac{(1+M)}{\beta^2}} \tag{6.8}$$

The current mirror gain is exactly equal to M when $\theta = \frac{(1+\beta)\cdot M-\beta}{\beta^2}$. M should be less than β and greater than β/(1+β) to satisfy the condition of 0<θ<1.

Similar to the design in Figure 6.6, process variations of β will result in a modest mirror gain error. The mirror gain error due to β variation is shown in Table 6.2.

Table 6.1: Current mirror (Figure 6.6) gain error due to process variation of β.

β	M	Mirror (Figure 6.6) gain Error (%)			
		-20%	+20%	-30%	+30%
15	13	1.63	0.78	3.09	1.00
	9	1.16	0.54	2.20	0.70
	5	0.65	0.30	1.25	0.39
	1	0.04	0.01	0.07	0.02
10	9	2.40	1.19	4.50	1.55
	5	1.40	0.67	2.65	0.87
	1	0.11	0.04	0.22	0.05
5	4	3.84	2.04	6.95	2.67
	3	2.98	1.54	5.45	2.01
	2	1.98	0.99	3.68	1.29
	1	0.65	0.29	1.28	0.36

From Table 6.2, we can see that, the worst case mirror gain error is 8.36% for β=5 and M=4. For M=1 and β=5, the error is 1.59%, which is slightly larger than what was achievable with the previous design.

6.5 Proposed Current Mirror With Multiple Outputs

To have multiple outputs, the current mirror shown in Figure 6.7 can be modified to a mirror with multiple outputs as shown in Figure 6.8.

If the mirror gain from the input to the outputs is nominally unity, the current mirror gain is given by the expression

Table 6.2: Current mirror (Figure 6.7) gain error due to process variation of β.

β	M	Mirror (Figure 6.7) gain Error (%)			
		-20%	+20%	-30%	+30%
15	13	1.76	0.82	3.35	1.05
	9	1.25	0.57	2.39	0.74
	5	0.70	0.32	1.36	0.41
	1	0.56	0.014	0.08	0.02
10	9	2.68	1.29	5.03	1.66
	5	1.56	0.73	2.99	0.93
	1	0.12	0.05	0.25	0.06
5	4	4.57	2.23	8.36	3.04
	3	3.57	1.77	6.62	2.29
	2	2.40	1.14	4.52	1.47
	1	0.80	0.33	1.59	0.42

$$A = \frac{I_{out1}}{I_{in}} = \frac{I_{out2}}{I_{in}} = \frac{\left[1 + \frac{N+1}{\beta} \cdot \theta + \frac{N+1}{\beta} \cdot \left(\frac{1}{N} - \theta\right) \cdot \frac{1}{(1+\beta)}\right]}{\left[1 + \frac{N+1}{\beta^2}\right]} \tag{6.9}$$

where N is the number of outputs of the current mirror.

The nominal current mirror gain is given by Equation (6.8)

The mirror current gain exactly equals to 1 if

$$\theta = \frac{N + (N-1) \cdot \beta}{N \cdot \beta^2} \tag{6.10}$$

To keep all branch current of emitter of Q5 positive, i.e.,

$$\frac{1}{N} - \theta > 0 \quad and \quad \theta > 0 \tag{6.11}$$

From (6.10) and (6.11), the maximum number of outputs N has to be less than β-1.

6.6 Conclusions

A new current mirror design based on a split-collector bipolar transistor was introduced and discussed in detail. The new design offers significant improvements in mirror gain accuracy over what is achievable with existing approaches in processes with low β transistors. Extensions of this structure in applications requiring high output impedance or multiple outputs were discussed also. This current mirror is particularly attractive for building current mirrors from lateral transistors in standard bipolar processes but can also be used with parasitic bipolar transistors in standard CMOS process

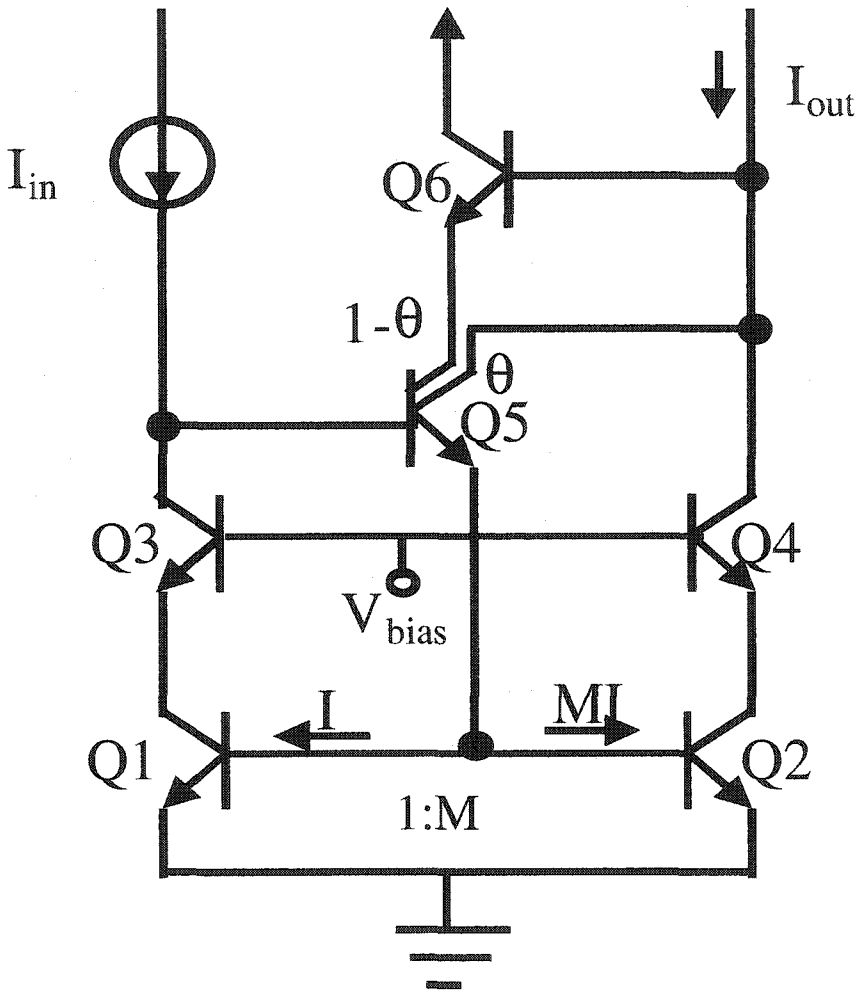


Figure 6.7: A cascode current mirror with split-collector to compensate for the base currents

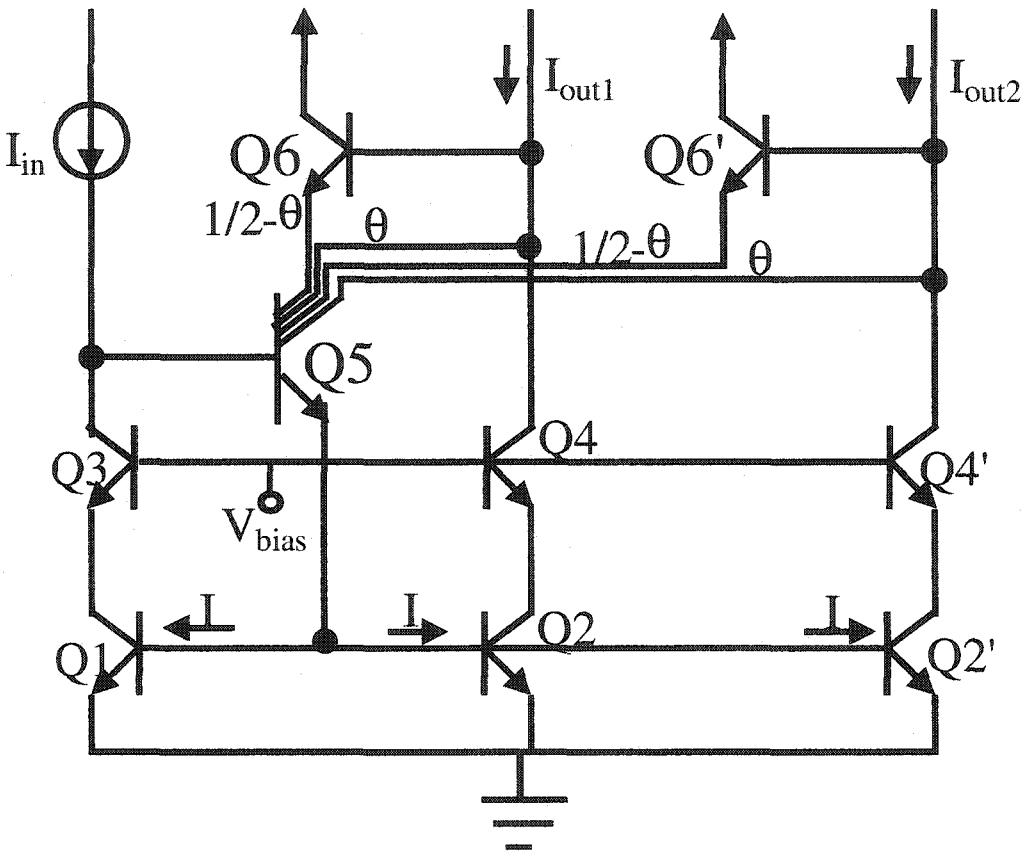


Figure 6.8: A current mirror with multiple outputs (for N=2, N is the number of outputs)

CHAPTER 7 GENERAL CONCLUSIONS

A high frequency voltage control oscillator with temperature and process compensation, a high-speed VCO-derived low-pass filter, a high-speed VCO-derived band-pass filter and a current mirror with accurate mirror gain for low β transistors are presented in this dissertation.

A temperature and process compensated VCO, which is designed to operate at 2 GHz, and whose frequency variation due to incoming data is limited in 1% of its center frequency, was presented. The simulation results show that the circuit has only a temperature and process variation of ±3.33% over fast and slow process corners and over the 0°C to 100 °C temperature range. This is a reduction of in excess of a factor of 10 when compared to a conventional VCO design. The test results show that, without process change presence, the frequency variation due to a temperature change over 0°C to 100 °C is around 1.1%. This is a reduction of a factor of 10 when compared to a conventional VCO.

A method of designing monolithic filters derived from CMOS VCOs was introduced. A sample of the VCO-derived low-pass filters and a sample of the band-pass filters were presented. A low-pass filter with a cut-off frequency of 4.3 GHz was designed in TSMC CMOS 0.25 μm process. It exhibits a THD of – 40dB with a 200mV single-end output swing. A band-pass filter with a center frequency tunable from 2.28 GHz to 3.11 GHz and a Q adjustable from 3 to 85 was also designed. It exhibits a THD of –40dB with an 80mV single-end output swing. The VCO-derived filters offer two main advantages over other types of integrated CMOS filters: higher operation frequency, and a higher and easily adjustable Q. VCO-derived filters offer potential for use in modern communication circuits that require modest distortion performance.

A new current mirror design based on a split-collector bipolar transistor was introduced that offers significant improvements in mirror gain accuracy over what is achievable with existing approaches in processes with low β transistors and discussed in detail. Extensions of this structure in applications requiring high output impedance or multiple outputs were discussed. This current mirror is particularly attractive for building

current mirrors from lateral transistors in standard bipolar processes but can also be used with parasitic bipolar transistors in standard CMOS process.

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